Silicon-Tungsten electromagnetic calorimeter

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HL e+e- colliders - FCCee, CEPC

Why PFA
- tag the boson through their di-jets decays (better use of the luminosity)
- be able to use the tau decays as a polarimeter (see Weinberg angle measurement from $A_e$ and $A_\tau$ at Z peak)
- be less sensitive to noise in the detector (particles have clean topological signature in calo)
- be able to use timing for particle ID (see M.Ruan presentation at CEPC workshop dec. 2018)

Why silicon
- PFA needs small pixels size, good S/N at MIP, good linearity, stability
- be able to read the energy deposited at high frequency (40 mHz – no slow pulse like in some scintillators)
- to run at Z peak with reasonable occupancy (very small pixels size with fast readout)

Tungsten-Silicon
- # people working on ECAL
- Silicon a good choice??
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Why silicon
- PFA needs small pixels size, good S/N at MIP for modest thickness, good linearity, stability
- be able to read the energy deposited at high frequency (40 mHz)
- to run at Z peak with reasonable occupancy (very small pixels size)

High granularity **ECAL** (longitudinal segmentation and small lateral size) **gives you for free**
(almost free ... TOT in ASICS or LGAD diodes)

- BX-ID for neutral (about few ps per shower... limitation from jitter on clock distr.)
- A particle ID for charged tracks from TOF (about 30 ps/layer)
HL e+e- colliders - FCCee, CEPC

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Why tungsten
- To have a good Moliere radius (about 2 cm)
- To have a modest total thickness (about 20-25 cm for 24X0 and 30 layers)

Known Problems
- The fragility and cost of the silicon wafers
- The mechanics and cost of tungsten
Information about the active device

<table>
<thead>
<tr>
<th></th>
<th>Np.e. /MIP</th>
<th>linearity</th>
<th>Longitudinal segmentation</th>
<th>Timing (ps) at mip</th>
<th>cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scintillator (3 mm &amp; SiPM)</td>
<td>10-20</td>
<td>&lt;1000 mip</td>
<td>***</td>
<td>?? (pb related to noise)</td>
<td>**</td>
</tr>
<tr>
<td>Silicon (300µm)</td>
<td>24000</td>
<td>No limit</td>
<td>***</td>
<td>30/(Nlayer) 1/2</td>
<td>*</td>
</tr>
<tr>
<td>Shashlik type</td>
<td>***</td>
<td>Yes</td>
<td>*</td>
<td>30</td>
<td>***</td>
</tr>
</tbody>
</table>

Good S/N @mip for <1mm thickness, timing measurement, small pixel size, .. → Silicon

Information about the radiator

<table>
<thead>
<tr>
<th></th>
<th>X0 (cm)</th>
<th>( \lambda_1 ) (cm)</th>
<th>Ratio</th>
<th>Molière Rad (cm)</th>
<th>Mechanics</th>
<th>cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fe</td>
<td>1.76</td>
<td>16.8</td>
<td>9.5</td>
<td>1.69</td>
<td>***</td>
<td>***</td>
</tr>
<tr>
<td>Cu</td>
<td>1.43</td>
<td>15.1</td>
<td>10.6</td>
<td>1.52</td>
<td>***</td>
<td>*</td>
</tr>
<tr>
<td>W</td>
<td>0.35</td>
<td>9.6</td>
<td>27.4</td>
<td>0.93</td>
<td>**</td>
<td>*</td>
</tr>
<tr>
<td>Pb</td>
<td>0.56</td>
<td>17.1</td>
<td>30.5</td>
<td>1.00</td>
<td>*</td>
<td>***</td>
</tr>
</tbody>
</table>

Good ratio, small Molière radius and good mechanical behaviour → Tungsten
With about 10-20 p.e. at mip and a large dynamics (>800 mip) a large S/N is very difficult if the signal is low (even with good SiPm)

Following electronics experts (Omega’s engineers*):

“For such a dynamic, the overall noise is about 2500 eENC (1500 for ASIC VFE intrinsic)”

- 2500 eENC for SKIROC2A and CALICE PCB/Detector
- 2500 eENC for HGROC(CMS) and about 5000 overall in TB, (readout 40 MHz)

\[
ENC = \sqrt{ENC_C^2 + ENC_I^2 + ENC_{Rp}^2 + ENC_{Rs}^2}
\]

* In charge of readout for ILD ECAL, ILD HCAL, HGCAL ECAL and HGCAL-HCAL
Running with high luminosity and cross section (Z peak)

Solution : Buffering

Study made for SiD at 250 GeV / ILC

KPiX Studies - Buffer Multiplicity

• Forward multiplicity might be more than 4 buffer KPiX (current design) could handle
  • Recent optimization studies indicate that 6 buffers will be adequate, taking into account all known processes.
• 6 buffers also improve fractional hit loss within detector at shower max and radially
• Must study KPiX to see if more buffers might be added while preserving architecture (preconceptional ideas only)

Arxiv: 1609.07816
**Requirements**

a) Calibration of O(50) millions channels and signal stability (*small syst. uncert. needs same response for all collisions*)

b) Capability to make zero suppress “in-situ” (*we don’t want to read empty pixel*)

c) Keep S/N ≥ 8-10 at MIP level and coherent noise under control (*limitation of the DAQ and it is not interesting to store noisy pixels*)

d) Multiplexing for the quantity of signal line out (*we don’t want to have 100M cables*)

e) Power and thermal management due to large number of channels (*we don’t want to burn our electronics readout*)

f) Keep the cost under control (*we want an affordable cost*)

---

**One set of answers**

a) Choose stable device (silicon) or control & monitor the signal stability (Scint. or Micromegas)

b) ADC & digital memory in readout chip, close to active layer. Read memories continuously WITH S/N > 8

c) i.e. Silicon PIN diodes .... AC/DC coupling, ground loop...

d) Large number of Channels/VFE ASIC... (KPIX, SKIROC), but only few readout line

e) reduced the number of channels → the power to dissipate (see later)

f) Reduce the overall surface or use lower cost active device (Micromegas, scintillator)

BUT warning versus point a) and c) . 10 years contacts with producers, defining wafers design which reduce the cost
ILC - (ILD or SID)
- a duty cycle of about 1% on electronics ... no need for active cooling
- a readout every 500 ns
- 26 layers for 24X0, cost estimation made by experts: cheaper than CMS ECAL

CMS HGCAL
- Readout every 25 ns, active cooling, large number of layers
- High level of radiation (10^{16} n/cm^2/year) ... variation of the gain of the diodes
- The pile-up mitigate the power of PFA

FCCee/CEPC
- Readout every 25 ns (hypothesis)
- No problem of radiation
- Need active cooling (It allows pixels size of 6x6 mm – see my presentation at CEPC workshop 2017)
- Small pixel allows time measurement/particle (like in ATLAS or CMS)
- Small pixel allows to run at Z Pole (occupancy)... to be studied !!
Sampling ECAL calorimeter projects based on silicon diodes.

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Overall design for e+e- collisions at 250GeV up to 370GeV

SiW+CFRC baseline choice for future Lepton Colliders:

- Tungsten as absorber material
  - $X_0 = 3.5\,\text{mm}$, $R_m = 9\,\text{mm}$, $\lambda_i = 96\,\text{mm}$
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design
  - Allows for ~any pixelisation
  - Robust technology
  - Excellent signal/noise ratio: $\geq 10$
  - Intrinsic stability (vs environment, aging)
  - Albeit expensive...

Particle Flow optimised calorimetry

- Standard requirements
  - Hermeticity, Resolution, Uniformity & Stability ($E$, $(\theta, \varphi)$, $t$)
- PFlow requirements:
  - Extremely high granularity
  - Compacity (density)
Optimisation - 1

ECAL Radius

![Cost vs Outer R of the tracker (m)]

![rms(E)/mean(E) vs R_{ECAL}^{inner} [mm]]
Going from 30 to 22 layers

- Reduction of cost; (small) reduction of $R_M$; increase of Energy resolution
  - “better separation at the expense of the intrinsic resolution”

Increasing the Si thickness to 725μm, if really feasible (next slide)

Energy resolution $\sigma(E)/E$:

- for 22 layers w.r.t. 30: $+16.8\%$
- with 725μm w.r.t 500μm : $-6.1\%$

ECal thickness = 190.1 mm (close to 185 mm of DBD).

- 22 layers = 14 layers with 2.8mm thickness
  + 8 layers with 5.6mm shared between structure and slabs.

Impact of the silicon thickness on the resolution:

The resolution goes like $\frac{E_{\text{22}}}{\sqrt{1 + \text{th.}}}$ where th. is the Si thickness in hundreds of microns.
Carbon fiber – Tungsten structure with Alveola to slide in the active layers.

No DEAD ZONE !!!

ECAL geometry

J.-C. Brient (LLR)
Geometry could be the one of ILD

20 to 30 readout layers and 20-24 Rad. Length within thickness<25 cm
- Wafers glued on one side of PCB
- VFE asics on the other side
- **Cooling on the VFE side**
W-Si ECAL team is LAL, LPNHE, LPSC, Omega, Kyushu, KEK and LLR

All labs are in the CALICE coll. but KEK

![Silicon pad for ILD ECAL](image1)

Intensive study ongoing mainly on electronics of large scale Sensor and readout concept mature enough

Long-life needed: reliability is crucial

![Wafers glued on PCB](image2)

Testing new slabs in CERN SPS

“Long slab”
**Detector test**

**Cumulated « Mip » spectrum**

**S/N = MPV / \sigma(Ped)**

**S_N summary (all slabs)**

<table>
<thead>
<tr>
<th>Summary</th>
<th>Entries</th>
<th>Mean</th>
<th>Std Dev</th>
<th>( x^2 / \text{ndf} )</th>
<th>Constant</th>
<th>Mean</th>
<th>Sigma</th>
</tr>
</thead>
<tbody>
<tr>
<td>Entries</td>
<td>6107</td>
<td>20.29</td>
<td>1.593</td>
<td>50.96 / 30</td>
<td>794.1 ± 13.0</td>
<td>20.28 ± 0.02</td>
<td>1.52 ± 0.02</td>
</tr>
</tbody>
</table>

**Single cell energy distribution for 3 GeV e\(^+\) beam w/o absorber**

**Width**  
- Width: 0.07935 ± 0.00003
- MP: 0.9629 ± 0.0403
- Area: 3.23 ± 0.01
- G(Sigma): 0.9886 ± 0.01103

**Width**  
- Width: 0.222 ± 0.005
- MP: 2.179 ± 0.003
- Area: 0.001 ± 0.005
- G(Sigma): 0.9956 ± 0.0015

**Energy (MIP)**
Layer=3, ASIC=0, channel=3

- signal (pedestal subtracted)
- pedestal (subtracted)

One pixel

MIP fit

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\chi^2$/ndf</td>
<td>55.75 / 56</td>
</tr>
<tr>
<td>Prob</td>
<td>0.4842</td>
</tr>
<tr>
<td>Width</td>
<td>4.884 ± 0.277</td>
</tr>
<tr>
<td>MP</td>
<td>60.18 ± 0.22</td>
</tr>
<tr>
<td>Area</td>
<td>3951 ± 79.7</td>
</tr>
<tr>
<td>GSigma</td>
<td>4.971 ± 0.459</td>
</tr>
</tbody>
</table>
1.6m long, almost the full scale for the final detector

**Analysis on going**
With a large dynamic and a large number of channels, it is important to have a good S/N (in order not to read noise at large, saturating the DAQ)

Test Beam in DESY – July 2018

Pixels at <30 cm from DAQ FPGA

Test Beam in DESY -2017

Pixels at 160 cm from DAQ FPGA

Landau response to electron mip

Just an extraction from logbook

preliminary
ECAL cooling studies

Passive cooling

(*ILC*)

Active Cooling

(*CEPC, FCCee or CLIC*)

Passive cooling ramp example

Passive cooling ramp set up test

Active cooling test layout (400mm x 300mm x 3mm thick copper plate with 1,8OD pipes embedded)

Active cooling set up test with water at room temperature

J.-C. Brient (LLR)
Passive cooling can lead to more compact solutions depending on the total power to extract and the acceptable temperature gradient.

Active cooling improves thermal field distribution and can extract much more heat.

It requires a qualified pipe insertion process.
Cooling test

Passive cooling

Active cooling

Thermal static FEA analysis thermal field example using ANSYS with 1W extracted

Comparison between thermal static analysis and theoretical approach

Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1.5mm ID pipe

J.-C. Brient (LLR)
Cooling test

Active cooling pipe insertion test with cold water

- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling.
Realistic (from CMS studies) cross section of the ECAL with active cooling:

- Copper cooling layer 3.5 mm
- PCB 1.6 mm
- Silicon wafers 0.75 mm + glue 0.05 mm
- Kapton HV 0.5 mm + glue 0.05 mm
- Tungsten 3 mm
- ASIC BGA 1 mm
- Cooling tube 2 mm

On average 9 mm/layer

All thicknesses are based on prototypes... (from ILD or from CMS)
No extrapolation

J.-C. Brient (LLR)
Happy with all the progresses, BUT

Standing problems
Hardware
- Readout VFE
- Readout at 1.7 m
- Clock distribution
- Signal at long distance
- Aging of the gluing (10 years checked)
- PCB production
- DIF card small size (4x3 cm)
- Power distribution, cooling distribution
- Definition of quality control and test...

Standing problems
Software
- more than 1 PFA reconstruction software
- Automatic calibration
- HL- Zero suppress
- etc...

Lot of things to do
PFA possible only if
(or more globally “jets”)
Optimising for a fantastic Vertex and Tracker ... and Forgetting the calorimeters
The future ECALs are more cameras than thermometers

Use particle flow Alg. Rec/ID of: $\gamma/e/u/jet/b$-jet/MET

All detectable particles leave traces in calorimeter

CMS HGCAL upgrade

Huaqiao Zhang @ HKUST  Jan 19, 2018
Instead to start from the hardware, I think the 2 detectors have to be optimized for different type of performances on physics results.

Before you asked for questions, I have one for the audience.

Why do we need 24X0?
CONCLUSION

ECAL for e+e- circular collider at from Z peak to 250 GeV

- Ultra granular calorimeter, optimized for PFA, would do the job at circular e+e- machines (including EW physics with tau, i.e. Higgs CP violation studies and at Z-pole)

- Active cooling: R&D for CMS demonstrate the feasibility for CEPC, FCCee

- Large luminosity and large number of pixels leads to a MANDATORY S/N>10 at MIP. This condition is fulfilled by ILD prototype, even at 1.6m from readout concentrator

**Silicon –tungsten meet the requirements**
Including the cost ... thanks to the upgrade of CMS, ATLAS.... We are talking of about a cost significantly lower than the crystal ECAL of CMS-ECAL.... it is no longer a good reason to say no to silicon

22 layers of 700 microns silicon wafers with 6x6 mm pixels size
BACKUP
On the near and mid-term future

Full prototype with about 20 layers at the end of 2018 .. mid/end 2019

- Test Beam (Data taking and analysis) 2019-2020
  (No beam at CERN, remains DESY (low energy) or FERMILAB)

- Going from ILC type to CEPC type. Cooling, pixels size, total rad. Length, etc...

- Going from prototype to “full scalable” (we have already 1.6m long detector slab)

- Interact with industry for optimized production and cost (tungsten, silicon, etc...)
  (amazing for me that HPK is the single producer in the world for high resistivity silicon wafers)

Transfer knowledge to students about ultra-granular calorimeter
(there is specific problems to this type of device.... Ask for to CMS 😊/😊)
Important to learn about with real hardware device... HGCAL can tell you

All groups interested, do not hesitate, contact us, there is work for all expertises
brient@llr.in2p3.fr
Detector SLAB (exploded view)

Active Sensor Unit (ASU)
Si+PCB+FE

Shielding (copper)

Cooling plate (copper)

H-Shaped structure (Tungsten/CFi)

Interface / layer (connectors)

Electronics VFE INSIDE
Efficient cost optimization is in progress
Optimisation with the number of Layers, the silicon thickness, a better use of the silicon ingot, the internal radius of the ECAL, etc ... about 40% reduction is expected by cost experts with modest impacts on performances (G4 full simulation.. Published in JINST)

The preliminary cost estimate is NOW at the level of 90% of CMS-ECAL
On the thermal dissipation

level of granularity can be afforded without powerpulsing (like at ILC)?

• For physics, the smaller is the best (it continue to improve largely even for \( S_{\text{Pixel}} \ll R_m \)) BUT for the electronics cost and cooling, … there is some limits

• Readout every 25 ns; no power pulsing
  readout frequency versus ILC x 14 (350 ns to 25 ns)
  \( \text{conso/cell} = 2.8 \text{ mW} \) (Analogic part SKIROC2 without PP) +
  2.1 mW (=0.15 x 14 for digital part with readout every 25 ns)

  \( \text{-------------} \)
  \( = 5 \text{mW} \) … Propose to use 10 mW/channel (including a safety factor of 2)

• From CMS upgrade project-\textbf{HGCAL}, active cooling system can be stabilized in temperature for about 100W/layer, with fluid running in tube inside cooper plate (\( R_m \) not so good than ILC… but)

Taking into account the chosen layer size (= 150x20 cm\(^2\)) and the 100W, The cooling can afford pixel size of about 0.6x0.6 cm\(^2\)!!! We have it
On the hermiticity

A possible detector geometry

Geometry “No dead zone”