Operational Experience with the DEPFET Based PXD Pixel Detector at Belle II and Possible Improvements Utilizing Micro-channel Cooling


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SuperKEKB at Tsukuba, Japan

- e+/e- collider, circumference ~3km, at Y(4s) resonance 10.58 GeV

- KEKB → SuperKEKB: 40x luminosity upgrade ("nano beam" scheme and 2x higher currents) \(2 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1} \rightarrow 80 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}\)
3 Commissioning phases

- Phase 1: 1st half 2016, circulating beams w/o Belle2, just BEAST 2
- Phase 2: spring 2018, first collisions, Belle 2 and part of VTX + BEAST 2 system for backg. monitoring \( \Rightarrow L \approx 10^{34} \text{ cm}^{-2}\text{s}^{-1} \)
- Phase 3: March 2019, final detector, final beam optics and collimators, gradual increase of the inst. luminosity \( \Rightarrow 80 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1} \)
Higher luminosity
- Higher event rate, higher background, higher radiation damage...

Detector upgrade → Belle II
- New PID components, upgraded CDC...
- New VXD: 4 layers DSSD + 2 DEPFET pixel layers
### Belle II PXD

<table>
<thead>
<tr>
<th></th>
<th>L1</th>
<th>L2</th>
</tr>
</thead>
<tbody>
<tr>
<td># ladders (modules)</td>
<td>8 (16)</td>
<td>12 (24)</td>
</tr>
<tr>
<td>Distance from IP (cm)</td>
<td>1.4</td>
<td>2.2</td>
</tr>
<tr>
<td>Thickness (μm)</td>
<td>75</td>
<td>75</td>
</tr>
<tr>
<td>#pixels/module</td>
<td>768x250</td>
<td>768x250</td>
</tr>
<tr>
<td># of address and r/o lines</td>
<td>192x1000</td>
<td>192x1000</td>
</tr>
<tr>
<td>Total no. of pixels</td>
<td>3.072x10^6</td>
<td>4.608x10^6</td>
</tr>
<tr>
<td>Pixel size (μm^2)</td>
<td>55x50, 60x50, 70x50, 85x50</td>
<td>55x50, 60x50, 70x50, 85x50</td>
</tr>
<tr>
<td>Frame/row rate</td>
<td>50kHz/10MHz</td>
<td>50kHz/10MHz</td>
</tr>
<tr>
<td>Sensitive Area (mm^2)</td>
<td>44.8x12.5</td>
<td>61.44x12.5</td>
</tr>
</tbody>
</table>

![Diagram of Belle II PXD](image-url)
The DEPFET all-silicon module

**DCDB** (Drain Current Digitizer)
- Amplification and digitization
  - UMC 180 nm
  - 256 input channels
  - 8-bit ADC per channel

**DHPT** (Data Handling Processor)
- First data compression
  - TSMC 65 nm
  - CM and pedestal correction
  - Data reduction (zero suppression)
  - Drives data link

**SwitcherB**
- AMS/IBM HVCMOS 180 nm
- Gate and Clear signal
- 32x2 channels

- **Pixel matrix operated in „rolling shutter” mode**
  - Only 4/768 rows active a time \(\rightarrow\) low power in active area

Material budget 0.21 %\(X_0\)

x-ray picture of fully assembled module
How to make thin DEPFETS

- thickness of the sensitive area is an almost free parameter
- full DEPFET technology in thin area
- thin area supported by a monolithically integrated silicon frame
Module assembly overview

Flip Chip of ASICs (~240°C):

- Bumped ASICs have the same solder balls (SnAg)
  - DHP bumping at TSMC, DCD bumping via Europractice
  - SWB bumping on chip level
- Flip Chip of PXD modules on custom made support plates

SMD placement (~200°C):

- Passive components (termination resistors, decoupling caps)
- Dispense solder paste/jetting of solder balls, pick, place and reflow

Kapton attachment (~170°C), wire bonding:

- Solder paste printing on kapton,
- Wire-bond, wedge-wedge, 32 µm Al bond wires
Quality control: Sensors and Modules

- Module substrate $\equiv$ DEPFET sensor and high density interconnect for the ASICs
  - Probe card testing of the sensitive part with temporary metal layer and probe card
  - Testing of the periphery of the sensor with “flying needles”

- Testing on module level in two steps
  - After flip-chip/SMD assembly with probe cards
  - Full characterization after kapton attachment
  - Rework (replacement of ASICs or kapton) possible!

- Probe card test statistics
  - 73 modules tested
  - 8 modules reworked
    - 7 with Switcher problems (flip-chip problem or broken Switcher)
    - 1 module had a non-functional DHP
  - Overall 97% yield after module assembly
Module characterization

- **71 modules** attached to pre-tested kapton cables
  - 40 modules needed for full PXD ...

- Collaborative effort (Bonn, Göttingen, HLL, MPP, Valencia)
  - Script based, automated procedure
  - Optimize/confirm ASIC and DEPFET parameters
    - Linear response of the ADC, high-speed
    - Off-module link of DHP
  - Charge collection (DEPFET voltages: Drift, HV, Clear-Off)

- Damage and repair after testing
  - 2 x kaptons revealed shorts (modules ok after kapton exchange)
  - 1 x module: mechanically damaged (can not be depleted)
  - 2 x modules: SwitcherB damaged at test
Belle II Phase 2

- One sector of VXD (SVD and PXD), 10% solid angle coverage
  - Plus BEAST2 (Belle II Exorcism for A STable beam)
    - FANGS: Hybrid silicon pixel detector with FE-I4 front end (Bonn)
    - CLAWS: Plastic scintillators with SiPM readout (MPP Munich)
    - Plume: Double sided CMOS pixel detector (Strasbourg)
    - In addition Diamond rad. monitor, $^3$He detector, TPC

- Goal: understand the machine background!

- Time line
  - Beam start: mid March 2018
  - First collisions: April 26, 2018
  - Beam stop: July 18, 2018

- Achievements
  - Integrated 0.5 fb$^{-1}$
  - Peak lumi at the end $\approx 5 \times 10^{33}$ cm$^{-2}$s$^{-1}$
  - Vertical beam size $<400$nm
PXD + SVD + BEAST2 = real beast
Installation
Module performance in the beam – peds. and noise

- Modules characterized before installation, optimization in the experiment
- DCD plays important role
  - Analogue cm correction and offset correction on pixel level helps to narrow the pedestal spread
- Pedestals are stable, noise around 100 e- ENC at full speed (20 µs/frame, ~100 ns/row)
Hit maps

- Hit maps taken at a physics run, threshold set to ~700 e-
- Flat distribution of hits over the sensors
- “b-grade” (<99% live pixels) with few missing rows or columns masked out
  - One off-module optical link broke after installation, was recovered after de-installation (bad fiber connection)
Signal/noise spectrum, vertexing performance

- Landau fit of cluster S/N distribution: SNR > 50, at threshold of ~7σ
  - Read-out at full speed and through full DAQ chain at 20µs/frame and ~100ns/row

- Hit efficiency depends on track parameters and cuts, in general 97% - 99%

- Unexpected low-energy photon peak around 10keV, most likely synchrotron radiation
Radiation effects due to background in phase 2

- TID $\rightarrow \Delta V_{th}$
  - Adjustment of the gate-on voltage “on the fly”
  - Pretty homogeneous radiation field, $V_{\text{gate, on}}$ segmentation not used

- S/N for mips (MPV) varies over the sensor: 48 ... 55
  - Gradient mostly along the gate/clear lines
  - Reason not completely clear, also seen before irradiation $\rightarrow$ not irradiation related $\rightarrow$ needs more investigation
Radiation effects due to background in phase 2

- TID $\rightarrow \Delta V_{th} \sim -1.4 \text{ V (L1)}$ and $-1 \text{ V (L2)}$
  - This would correspond to about 1 to 4 kGy based on results from previous DEPFET irradiations
  - After $V_{\text{gate}}$ compensation, no effect on sensor performance

- Discrepancy to TID from diamond radiation sensors by a factor 10..100
  - Diamonds less sensitive to low-E x-rays, confirmed by TID seen from radio-chromic foils.
    - Also, the diamonds are at different place....
  - Source of this background not yet fully understood, investigations will be continued during phase3...
Join two modules to a ladder → “gluing”

V-grooves for small ceramic inserts on the back side → Reinforcement of the joint

**Yield issue:** out of 17 assembled ladders, 5 were lost due to particles and other mistakes

**Install de-scoped PXD** to meet the schedule for the start of phase 3 (March 2019)

- Full L1 (8 ladders) and 2/12 ladders in L2

First physics runs and luminosity ramp up of Belle II with this pre-version of PXD
Main feature: Modules are not upside down anymore. Insert the ceramic stiffeners from below after the glue dispense as before. All other steps remain mostly unchanged but the sensor surface is not touched anymore.

Tests, evaluation and optimization is ongoing

Preparation of a full fresh PXD for installation summer 2020 started...
Summary: Belle II PXD performance and status

- Assembly and testing of DEPFET PXD modules accomplished
  - Final yield >95%
- A sector of the PXD was successfully operated in Belle II
  - 10% of final installation
- Excellent performance of the modules
  - S/N > 50, almost spectroscopic quality, tracking efficiency >97%
- Background in phase 2 higher than anticipated from simulations
  - 15x for LER, 600x for HER
- SuperKEKB Phase 3: de-scoped for the start of phase3 PXD with 10/20 ladders installed
  - Commissioning together with SVD finished → installation of VXD done → **phase3 start 03/2019**
- Preparations for full replacement PXD in summer 2020 ongoing
Thermal management at Belle II PXD

- Belle II PXD cooling qualified on full thermal mockup
  - 9W/half ladder → 360W in total
  - Active (CO₂) cooling at EOS, SCB cooling block at -30°C
  - N₂ flow through SCB 20 l/min for sensitive region
    → r/o electronics ~20°C, sensor ~30°C

- Large deltaT between CO₂ and r/o
- SCB: lot of material (outside acceptance)

How to remove the heat more efficiently and with less material?

→ micro-channel cooling
Integrated micro-channels

A spin-off of SOI approach: thinned all-silicon module with integ. cooling

- idea: integrate channels into handle wafer beneath the ASICs
- channels etched before wafer bonding → cavity SOI (C-SOI)
- full processing on C-SOI, thinning of sensitive area
- micro-channels accessible only after cutting

Small team (Uni Bonn, MPG HLL Munich, IFIC Valencia), within the framework of AIDA 2020
First prototypes with integrated resistive heaters

DRIE etching of handle wafer

Module after cutting

Detail: inlet for the cooling fluid

CSOI wafer with integrated resistors

~350 µm
The interconnect challenge

- In-plane supply of the cooling liquid
  - 3D printed adapters also for mechanical support
  - Self-aligned to channel openings
  - Initial simple approach: „gluing“

- to standard fittings
- to PEEK tubes
Very simple test setup

- DEPFET operating temperature well above 0°C → *mono-phase fluid* is chosen (H₂O)
- Controlled environment to quantify cooling performance. *Room temperature stable at 25°C*
- Continuous operation for weeks without *leaks or clogging*
EOS cooling performance

- Low flow rate (~1l/h) and low pressure (<1bar) are enough to remove the heat generated in the front end
- Maximum power dissipation for a ΔT of 10 K as a function of the flow rate
  - Temperature stable up to a power density of 25 W/cm²
  - To remove 22W at the end of stave 3l/h are needed for a ΔT of 10K
  - Still low pressure: up to 1.5 bar
- Good agreement with the FE simulation within an error of 10%
Sensor cooling performance

- Micro-channels under the front-end and gentle air flow on the sensor part
  - Micro-channels don’t cool sensor (of course!)
  - Sensor cooling (incl. Switchers) require gas flow
Next steps

➤ Improve fluidics, temperature homogeneity, flip-chip to micro-channel area .... More to come, stay tuned
Summary

Thanks for your attention
Current ladder assembly sequence I

- **Step 1:** Modules have to be turned over, upside down
  - Module is held by vacuum through porous ceramic

- **Step 2:** Apply adhesive at the edge (dispenser)

- **Step 3:** Place on alignment stages, align

- **Step 4:** Place ceramic inserts, cure
Current ladder assembly sequence II

- **Step 5:** After adhesive curing at RT, the ladder is picked up from the alignment stages by ladder jigs

- Many details skipped, just pointing out main steps, there are of course many in-between...
Ladder assembly experience

<table>
<thead>
<tr>
<th>Ladder #</th>
<th>Layer</th>
<th>Status after assembly, failure mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>1</td>
<td>Okay → phase3</td>
</tr>
<tr>
<td>15</td>
<td>1</td>
<td>Okay → phase3</td>
</tr>
<tr>
<td>16</td>
<td>1</td>
<td>Particle problem at step 1 (then crack at EOS at HS assembly)</td>
</tr>
<tr>
<td>17</td>
<td>1</td>
<td>Okay → phase3</td>
</tr>
<tr>
<td>18</td>
<td>1</td>
<td>Okay → phase3</td>
</tr>
<tr>
<td>19</td>
<td>1</td>
<td>Okay → phase3</td>
</tr>
<tr>
<td>20</td>
<td>1</td>
<td>Okay → phase3</td>
</tr>
<tr>
<td>21</td>
<td>1</td>
<td>Okay → damaged on test bench (overheating)</td>
</tr>
<tr>
<td>22</td>
<td>2</td>
<td>one module broke at step 5, operator error (wrong setup)</td>
</tr>
<tr>
<td>24</td>
<td>2</td>
<td>Particle problem at step 1</td>
</tr>
<tr>
<td>28</td>
<td>1</td>
<td>Okay → phase3</td>
</tr>
<tr>
<td>29</td>
<td>2</td>
<td>Okay → phase3</td>
</tr>
<tr>
<td>30</td>
<td>1</td>
<td>Particle problem at step 1, and operator error (screw driver)</td>
</tr>
<tr>
<td>34</td>
<td>2</td>
<td>Okay → phase3</td>
</tr>
<tr>
<td>35</td>
<td>1</td>
<td>Assembly visually ok, but SWB damaged at or after assembly</td>
</tr>
<tr>
<td>36</td>
<td>1</td>
<td>Okay → phase3</td>
</tr>
<tr>
<td>37</td>
<td>1</td>
<td>Okay → spare at KEK</td>
</tr>
</tbody>
</table>
Failure classes during ladder assembly

▷ Operator mistake:
  ▷ Slipped screwdriver hitting the sensor through a small opening in the cover ....
  ▷ Use of the second, not yet fully qualified alignment set

▷ Damage during testing
  ▷ Overheating (kapton de-soldering) due to bad thermal contact of the EOS (faulty jig..)
  ▷ failure of L1_035 Switcher also possibly caused by testing, though not yet verified

▷ Particle problem
  ▷ At step 1, the sensor is face down pressed by vacuum onto the ceramic
  ▷ Though passivated, the sensor surface can be scratched leading to shorts in the metal system
  ▷ Various trials to manage the particle problem, the latest attempt was the introduction of a nylon mesh between sensor and vacuum jig
    ▷ Though it seems to be very efficient, it introduces even more assembly steps and higher risk of damage due to operator error
Ladder assembly strategy for PXD2020

- Change as little as possible!
- Don’t touch the sensor surface at all and reduce the number of handling steps

Modified assembly sequence (see next slide)

- Improve cleanliness of modules, jigs and assembly room
- Add more manpower

Proposal:
Install the process at HLL controlled CR (~ISO 6/class 1000)
Add another HLL technician

- Improve quality control

Introduction of an Assembly Control Group
More Sensors!!! Actually only for L1…. → PXD9-20 and -21

- Modules for 14 L2 Ladders are ready for ladder assembly, should be enough for PXD 2020

- Sensors left from the current production (can be seen as backup)
  - B-grade sensors: 1 L1-fwd, 6 L2-fwd, 1 L2-bwd, 2 L1-bwd → ready for assembly
  - With possible matrix shorts: 2 L1-fwd, 4 L2-fwd, 0 L2-bwd, 1 L1-bwd → tbc

<table>
<thead>
<tr>
<th></th>
<th>IF</th>
<th>OF</th>
<th>OB</th>
<th>IB</th>
<th>total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final modules</td>
<td>15</td>
<td>22</td>
<td>20</td>
<td>14</td>
<td>71</td>
</tr>
<tr>
<td>Final-P2 modules</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>Prototype modules</td>
<td>2</td>
<td>3</td>
<td>5</td>
<td>4</td>
<td>14</td>
</tr>
<tr>
<td>EMCM assemblies</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>12</td>
</tr>
<tr>
<td>used dummies (mostly ladder assembly…)</td>
<td>7</td>
<td>10</td>
<td>9</td>
<td>7</td>
<td>33</td>
</tr>
<tr>
<td>stock - not usable</td>
<td>5</td>
<td>24</td>
<td>30</td>
<td>3</td>
<td>62</td>
</tr>
<tr>
<td>stock - b-grade</td>
<td>1(+2)</td>
<td>6(+4)</td>
<td>1(+0)</td>
<td>2(+1)</td>
<td>10(+6)</td>
</tr>
</tbody>
</table>

- PXD9-20: 7+x wafers, PXD9-21: 12 wafers

- Have to assemble new modules: 12+12 IF and IB (including 50% spares and contingency) to complete new PXD 2020
Module assembly and testing

- **Flip chip**
  - Very good yield at IZM
  - Expensive (about 40k for phase3), difficult logistics
  - Meanwhile technology also at HLL, but in order to meet the schedule I would propose to use this service again
  - Do x-ray with filters at HLL; rework, if needed, can be done at HLL (technology available)

- **SMD at HLL**
  - No change, 100% yield so far

- **Probe card testing at HLL (have to re-install)**
  - Fast feedback to module production and rework at HLL

- **Kapton**
  - New kapton ordering, QC at MPP → agreed
  - Kapton soldering and wire bonding at MPP?
    - Very few failures, but some residues after vapour phase soldering → improvements?
Preparation for PXD2020 - ASICs

- **DHPT1.2b (Bonn)**
  - Need ~100 ASICs for L1 including 50% spares
  - Currently available at Bonn: 252 tested and 300 untested → 2x safety, if needed can test more

- **DCDB4.2 (KIT)**
  - Need ~100 ASICs for L1 including 50% spares
  - Available at KIT: 800 untested chips
  - KIT agreed to test the required number of chips, not critical

- **SwitcherB18v2.2 (KIT)**
  - Need ~150 ASICs for L1 including 50% spares
  - Slightly improved version of the currently used SwitcherB18v2.1
    - Reduced power in $V_{\text{sub}}$ node
    - Clamp circuit added between $V_{\text{dd}}$ and GND and between $V_{\text{ddRef}}$ and $V_{\text{SUB}}$
    - Changes in termination to allow default operation without JTAG
  - Two wafers with about 200 chips in total are currently at IZM for bumping and dicing
  - Another two wafers as backup
  - **Test and evaluation of the new features on hybrid level early next year**
  - Series testing of the chips agreed with KIT
Characterization
- Again collaborative effort: Bonn, DESY, GOE, HLL, MPP
- Need to keep setups and expertise alive over the next 1.5 years!
- This will be a major effort again, have to schedule the availability of the experts

Ladder Assembly MPP @HLL (if accepted)
- Develop procedure at MPP
- Install at HLL, assembly to be done by two technicians (HLL/MPP) in HLL CR (~ ISO6/Class 1000)

HS Assembly at MPP in the room where the ladder gluing was done up to now

Other items to be prepared in the coming ~6 months
- SCB assemblies
- PPs with inner cables
- Assemble the remaining modules from current sensor batch as soon as Switchers available
- ...
Main task for the VXD: time dependent CP violation

\[ e^+e^- \rightarrow \Upsilon(4S) \rightarrow B^0\bar{B}^0 \]

- Reconstruct the decay vertex of the \( B/\bar{B} \) meson pair
  - Measure differences in lifetime

- High precision vertexing required

- High resolution pixel layers close to the IP, L1 is crucial for resolution
  - Most low-E secondary particles \( \rightarrow \) very low material budget mandatory
IR movie – just as entertainment