International Linear Collider

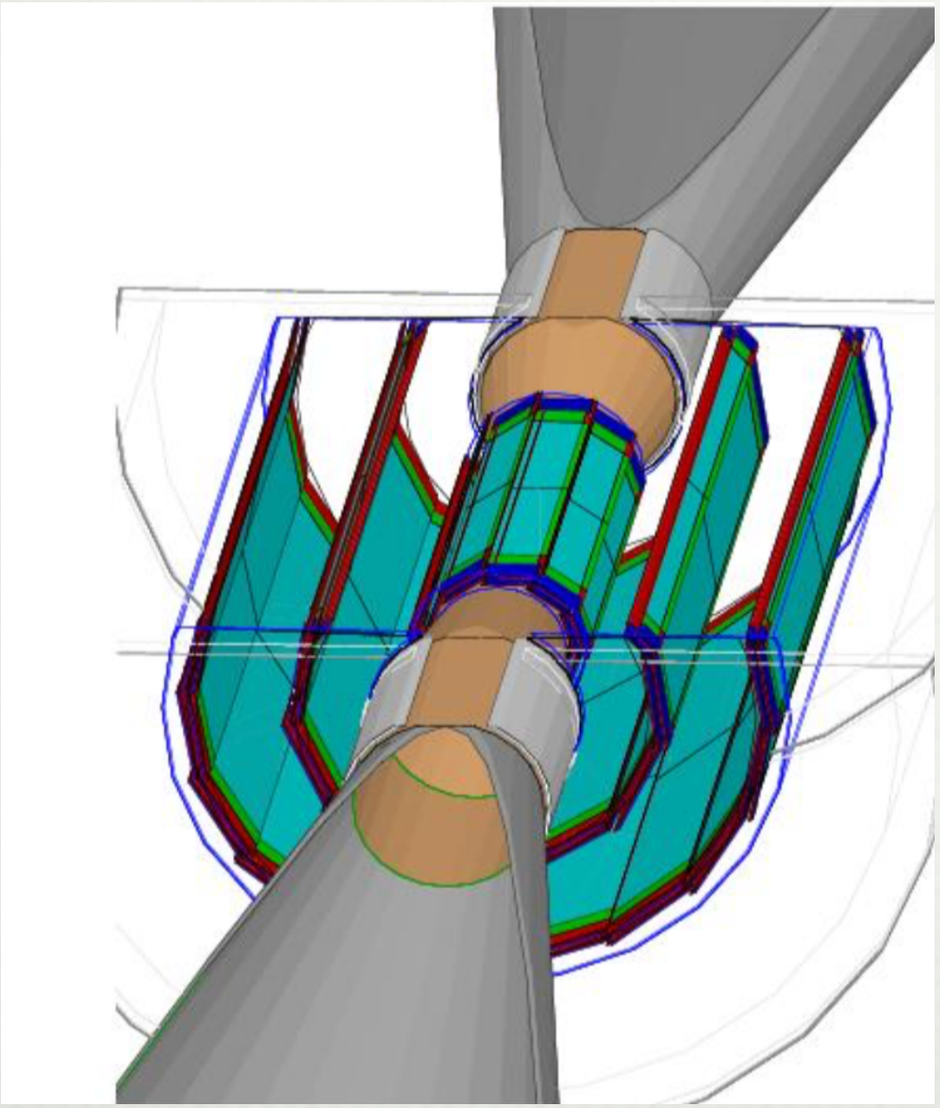
VTX-ing at the ILC experiments

HKUST
IAS program on HEP
Hong Kong, 19th January 2016

Massimo Caccia - Uni. Insubria - Como & INFN-Milano

The essence of vertex detection & reconstruction at the ILC experiments:

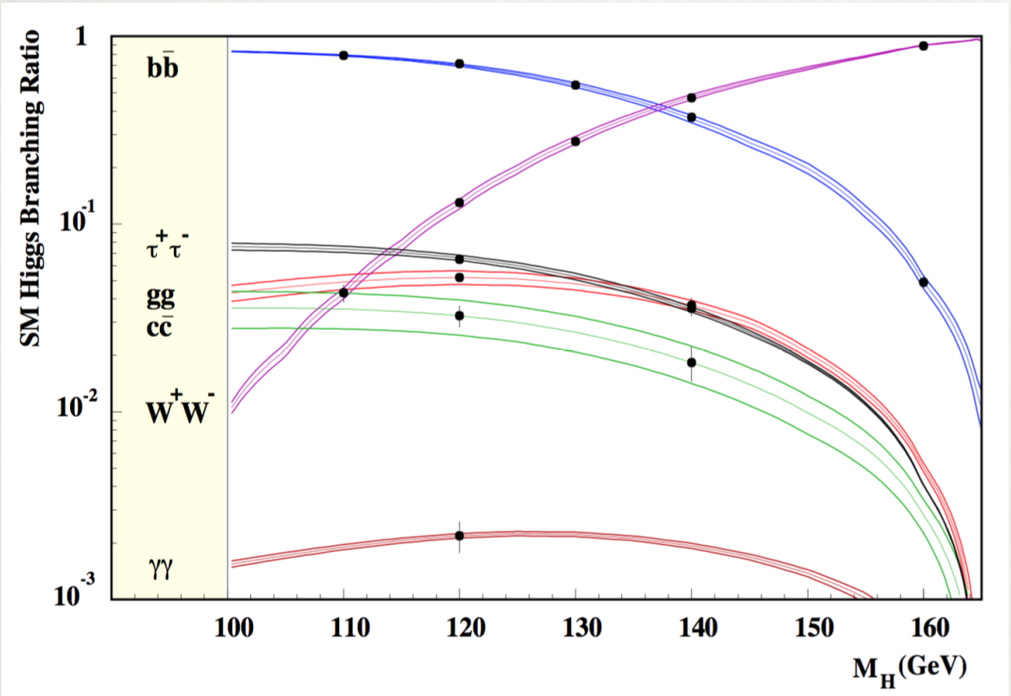
fit 1 GigaPixel in a Diet Coke can & keep it cool!



An artist's view of the VTX detector at the ILD

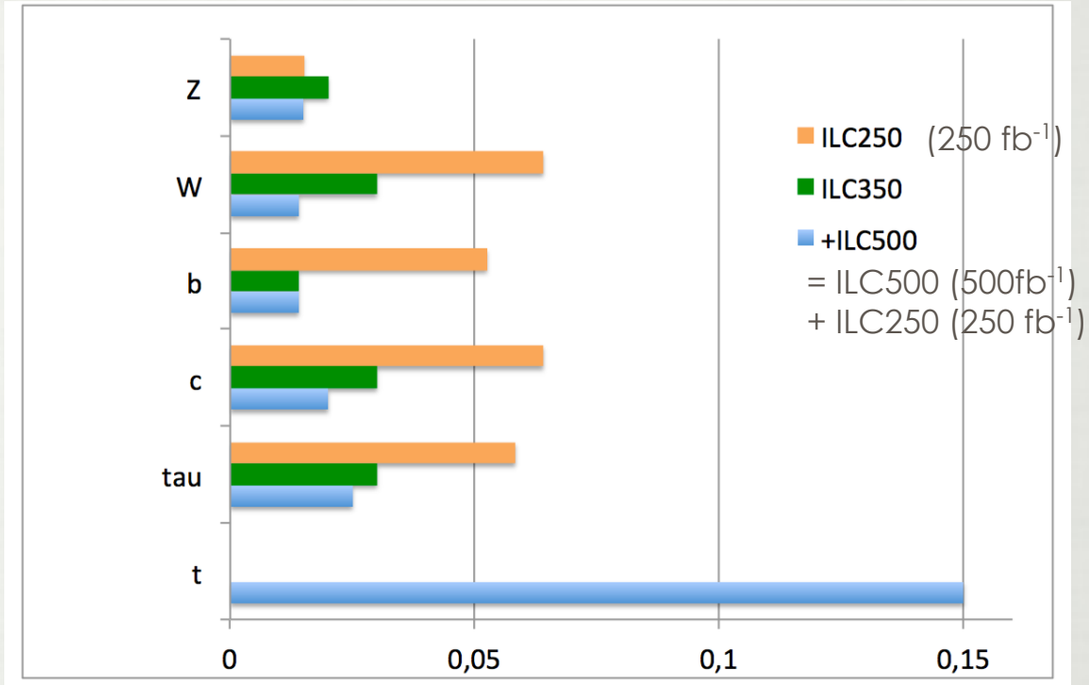
Barrel system						
System	R(in)	R(out)	z /mm	comments		
VTX	16	60	125	3 double layers	Silicon pixel sensors,	
				layer 1:	layer 2:	layer 3-6
				$\sigma < 3\mu m$	$\sigma < 6\mu m$	$\sigma < 4\mu m$
Silicon						
- SIT	153	300	644	2 silicon strip layers	$\sigma = 7\mu m$	
- SET	1811		2300	2 silicon strip layers	$\sigma = 7\mu m$	
- TPC	330	1808	2350	MPGD readout	$1 \times 6\text{mm}^2$ pads	$\sigma = 60\mu m$ at zero drift
ECAL	1843	2028	2350	W absorber	SIECAL	30 Silicon sensor layers, 5×5 mm^2 cells
					EcECAL	30 Scintillator layers, 5×45 mm^2 strips
HCAL	2058	3410	2350	Fe absorber	AHCAL	48 Scintillator layers, 3×3cm^2 cells
					SDHCAL	48 Gas RPC layers, 1×1 cm^2 cells
Coil	3440	4400	3950	3.5 T field	2λ	
Muon	4450	7755	280	14 scintillator layers		

M. Battaglia, ILC Reference Design Report, 2007



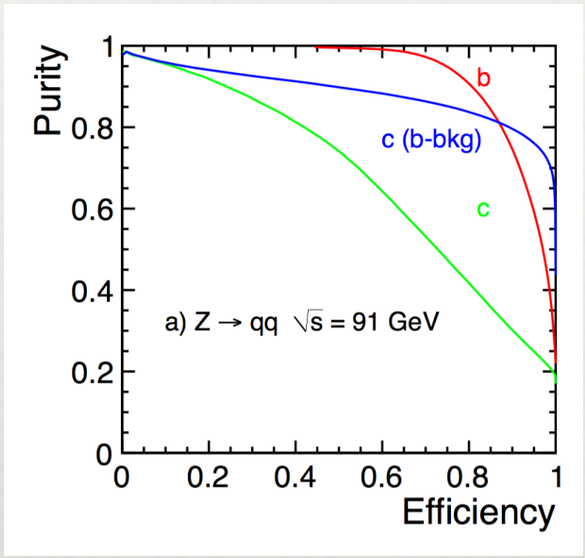
Br and expected sensitivity
(500 fb^{-1} @350 GeV)

K. Desch, Bellagio workshop 2012, LC Krakow report



Relative error of the Higgs couplings

Flavour Tagging

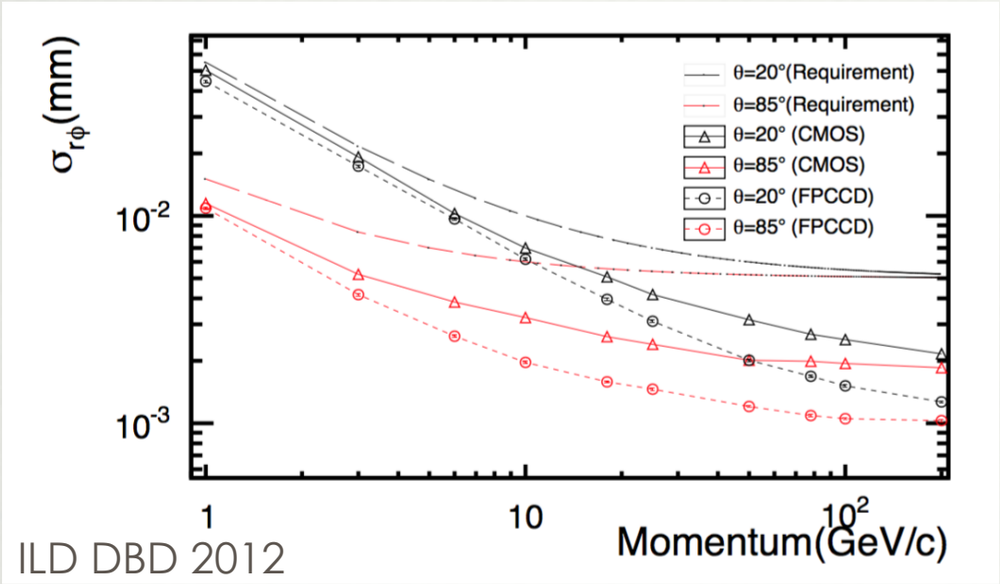


blue points relate to the sub-class of events with b quarks around
(b vs c mis-identification)

ILD Detailed Baseline Design 2012

To get to these Flavour Tagging Performance you have to start by single tracks:

- impact parameter resolution



ILD DBD 2012

$$\sigma_{ip} = a \oplus \frac{b}{p \cdot \sin^{3/2}\theta}$$

Accelerator	a [μm]	b [μm·GeV/c]
LEP	25	70
SLC	8	33
LHC	12	70
RHIC-II	13	19
ILC	< 5	< 10

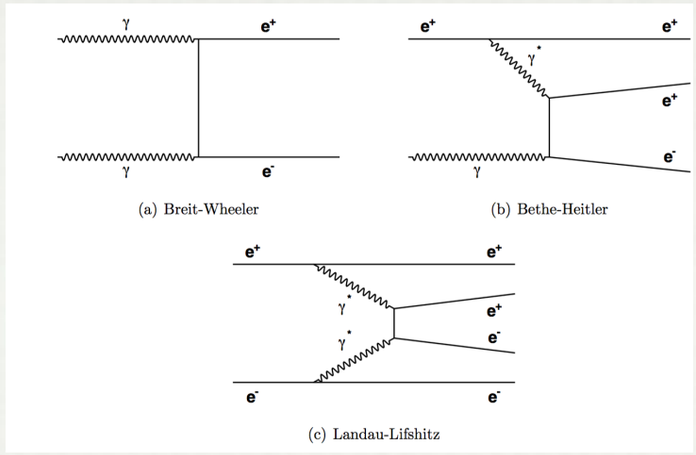
ILD LOI 2009

- a depends on the single point resolution and the ratio between the innermost radius and the lever arm:
  => σ_{sp} = 3 μm when R_{in} =16 mm and R_{out} = 60 mm

- b depends on the multiple scattering at the innermost radius:
  => thickness/layer = 0.15% X_0 [X_0 = 9.37 cm for Silicon]

- BE PRECISE 
- BE SLIM 
- AND GET CLOSE (to the i.p.)

✱ preserve the Pattern Recognition capability

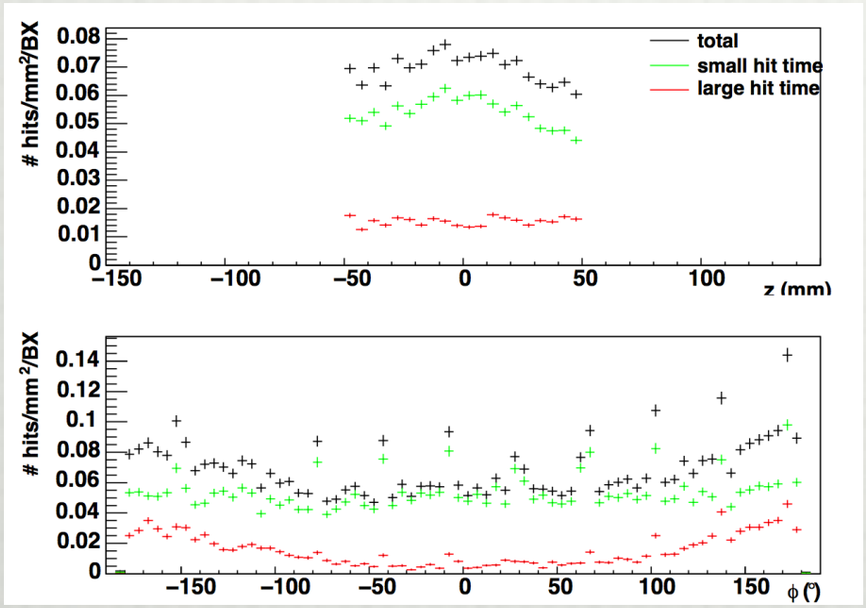


mind the Beamstrahlung pair production!

- BE SHARP!

hit rate in the first layer of the VD

occupancy ~10^{-2} /50 μs



DeMasi, Winter, ArXiv: 0902.2707v1

hit rate in the six layers of the ILD-VD

Layer	1	2	3	4	5	6
0.5 TeV	6.3±1.8	4.0±1.2	0.25±0.11	0.21±0.09	0.05±0.03	0.04±0.03
1 TeV	11.8±1.0	7.5±0.7	0.43±0.13	0.36±0.11	0.09±0.04	0.08±0.04

M. Winter, ALCW 2015

- BE FAST!
- BUT KEEP COOL!

And being precise, slim, sharp, fast & cool at the same time may not be easy

[even if you can relax at least on being (radiation) tolerant (1 kGy & 1011 n_{eq}/cm^2 per annum)]

- there are problems with more than ONE solution
- there are many ways to draw a nice tree
- and there is certainly more than one way to design a fair VD compliant with the specified boundary conditions:

Monolithic Active Pixel Sensors(MAPS)

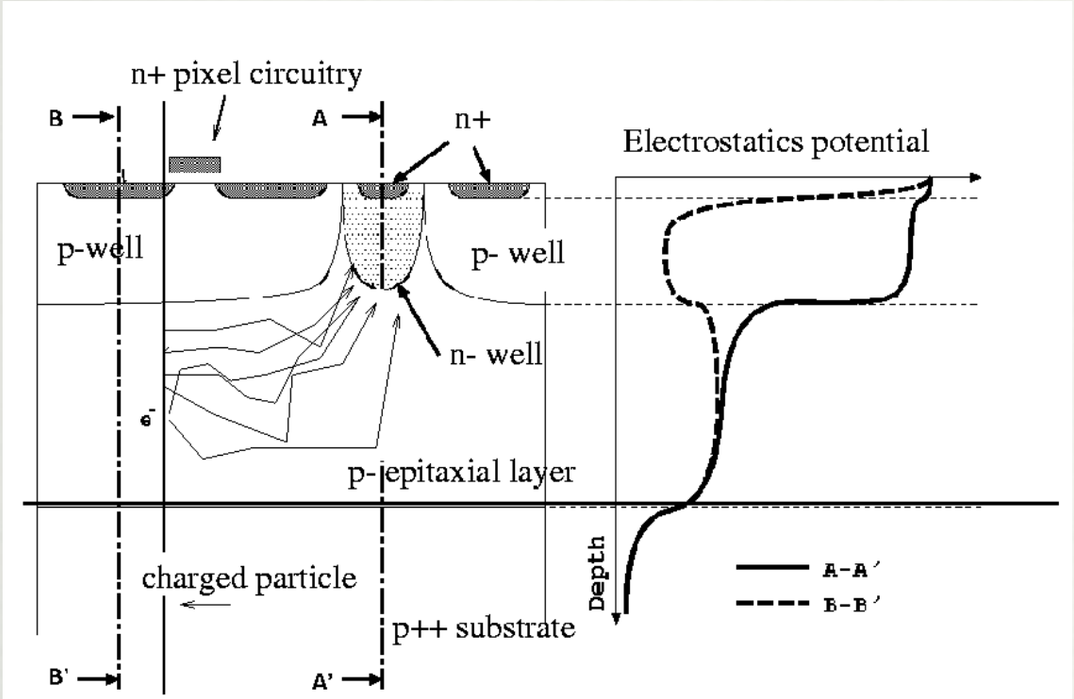
- MIMOSA
- CHRONOPIX
- ALPIDE
- else..

DEPFET

Fully Depleted SOI

CCD

MONOLITHIC ACTIVE PIXEL SENSORS



CMOS sensors for particle detection

- Main drive from digital cameras
- Pioneered @ LEPSI Strasbourg in the late 90's:
  - G. Deptuch at al, IEEE-TNS 49 (2002) 601
  - R. Turchetta et al, NIM A458 (2001) 677

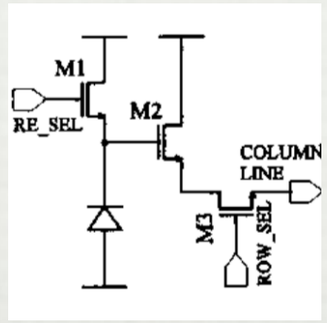
NON STANDARD SENSORS:

- based on the charge carrier generated in the epitaxial layer [2-14 μm thick, depending on the technology => SMALL signal (~80 e-h pairs/ μm)]

- diffusion detector vs [standard] drift sensors (the sensitive volume is NOT depleted => charge cluster spread over ~ 100 μm [10 μm] AND collection over ~ 150 ns [10 ns])

NEVERTHELESS OFFERING SEVERAL ADVANTAGES:

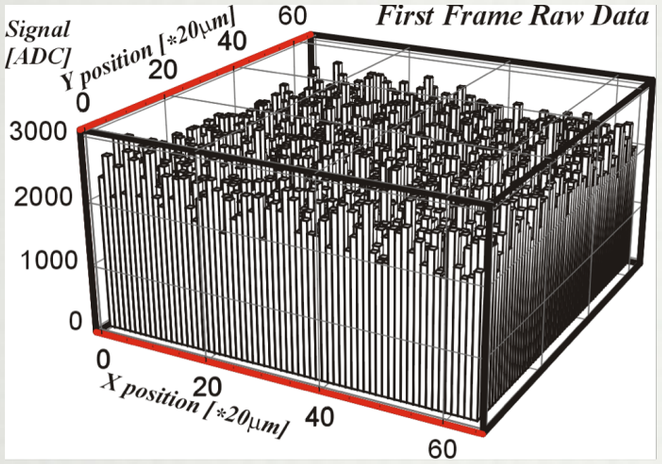
- very simple baseline architecture (3Transistors: reset, source follower, address key)

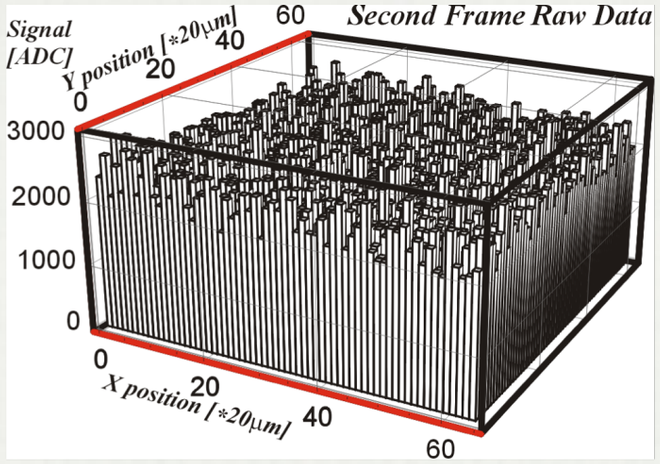


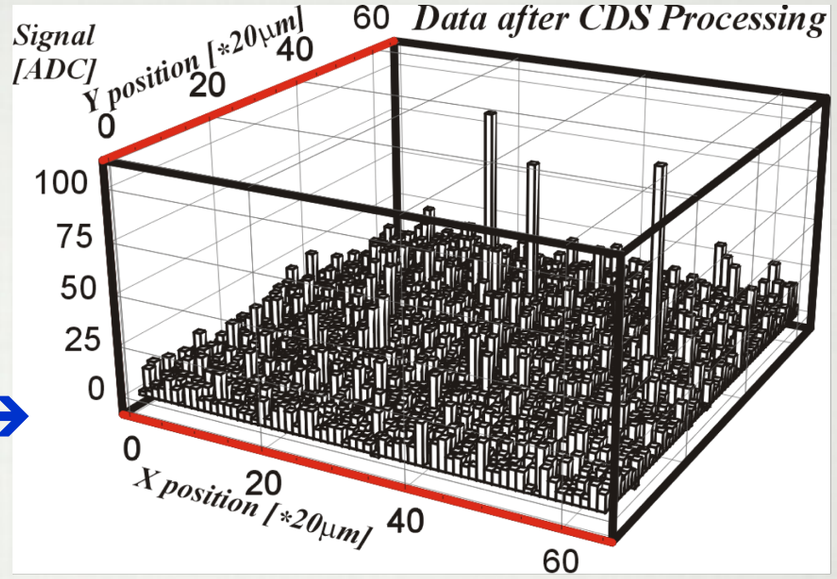
- standard, well established industrial fabrication process, granting a cost-effective access to state-of-the-art technologies

☑ **Signal identification** (courtesy of W. Dulinski, LEPSI Strasbourg):

1. The Correlated Double Sampling:

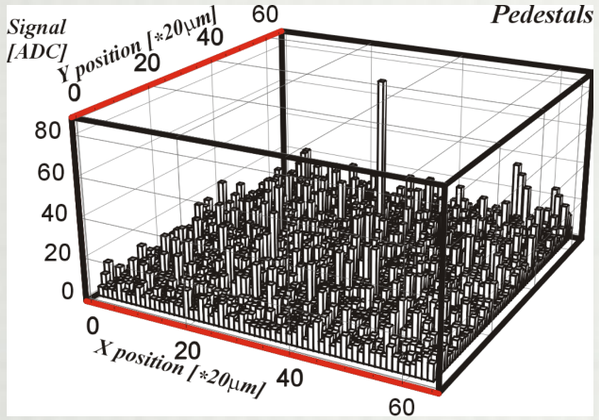


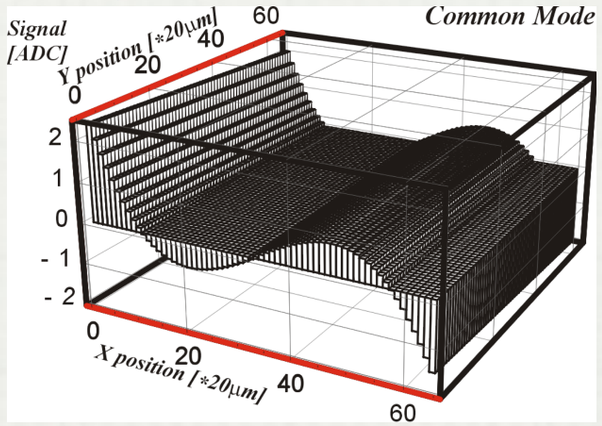


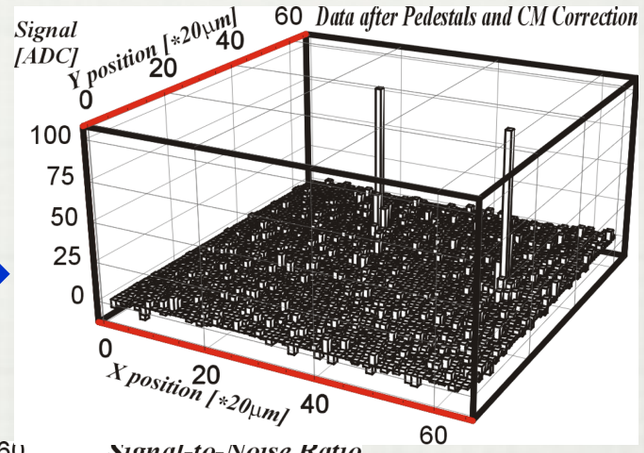


frame2 – frame1)

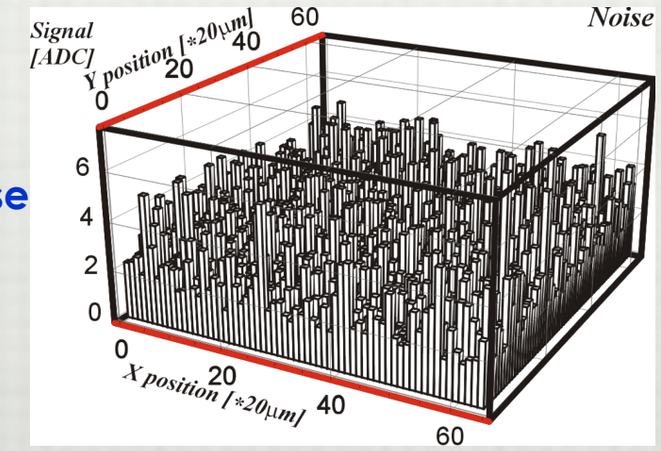
2. Subtract pedestals (due to leakage current) & Common mode

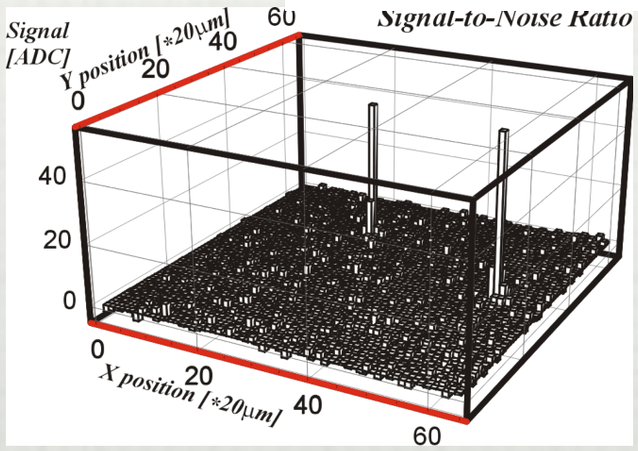






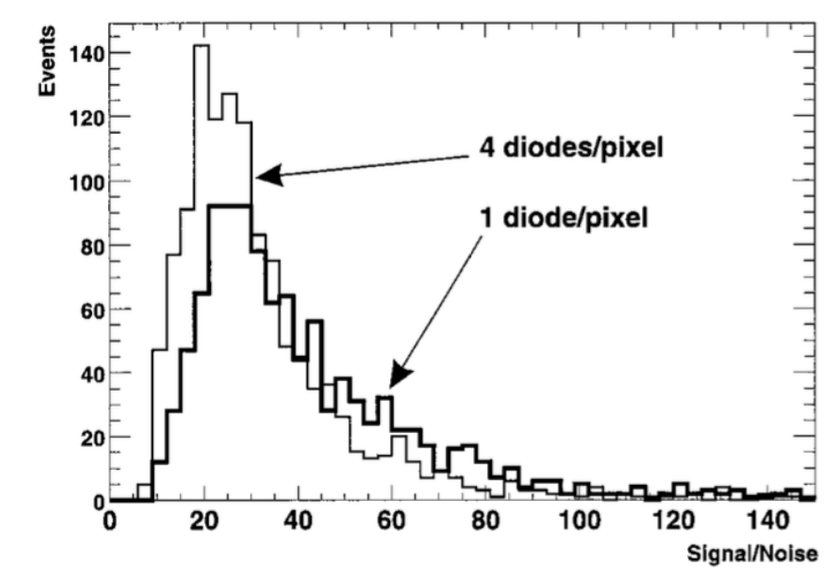
3. Evaluate the candidates against the noise (r.m.s of the pedestal distribution)



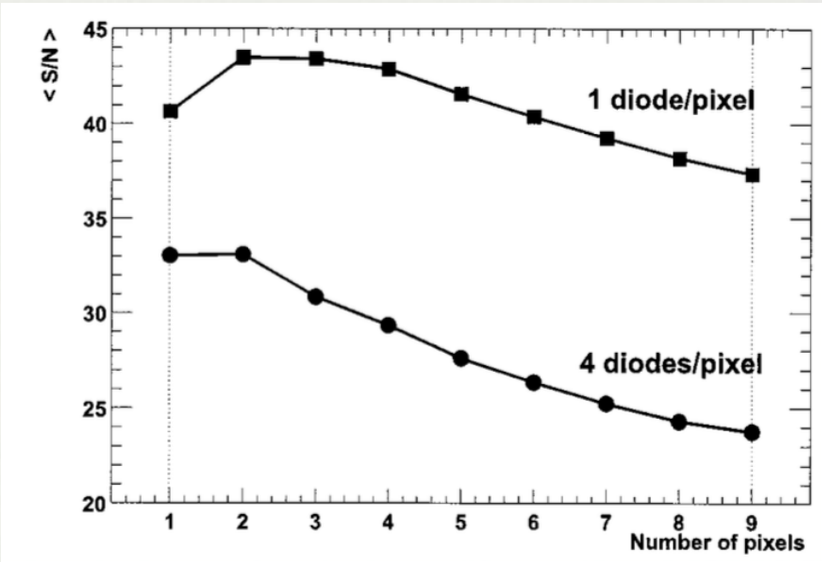


Signal-to-noise ratio evaluated for considered event

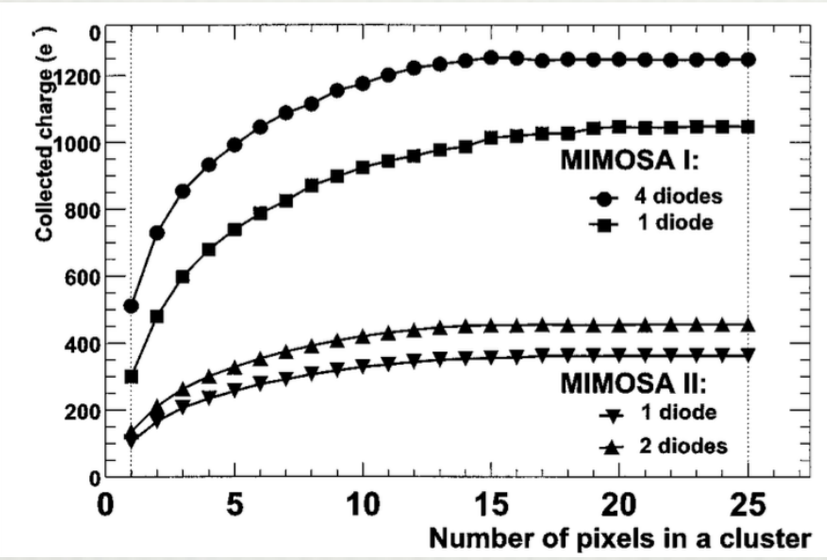
A tribute to the Strasbourg team; early results from the MIMOSA (Minimum Ionising particle MOS Active pixel sensors) 1 & 2 (back to 2002):



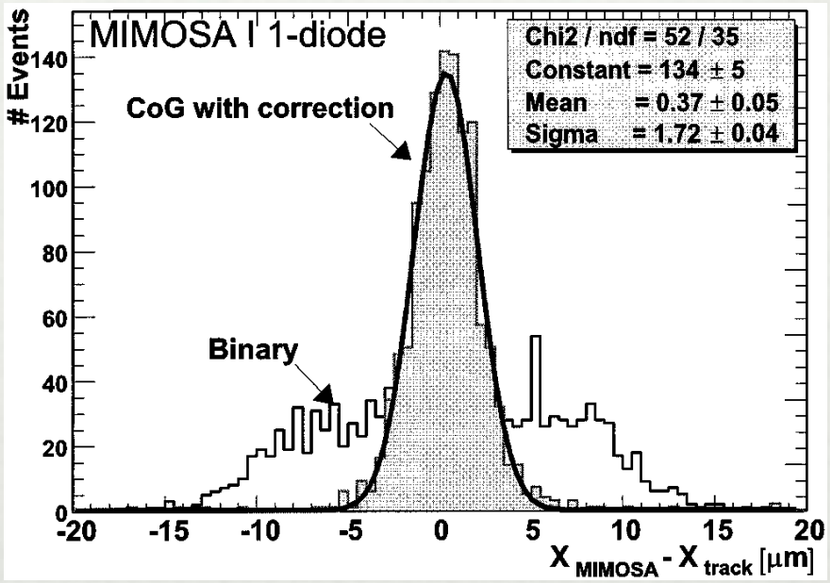
S/N for the seed pixel



S/N vs cluster size



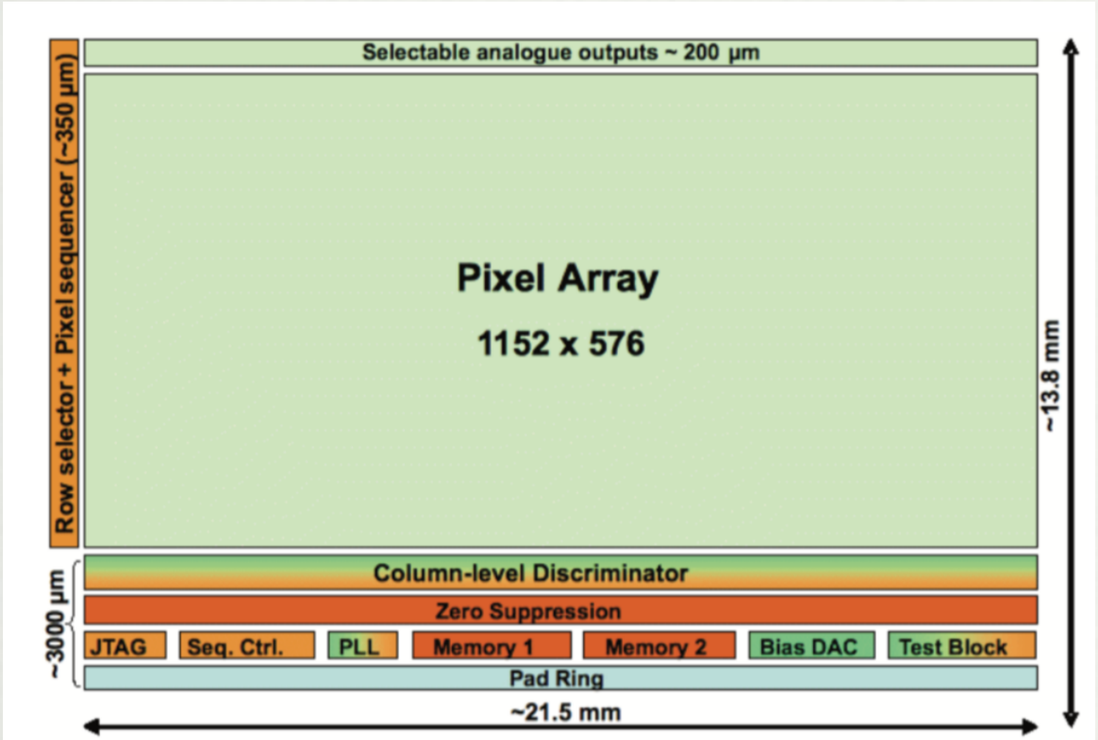
Collected charge vs no. pixels



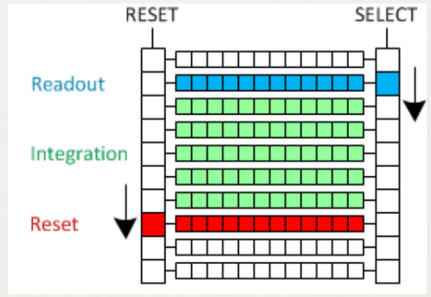
Resolution

AMS 0.6 μm technology - 14 μm epitaxial layer - 20 μm pixel pitch

The MIMOSA26, the baseline architecture for the high spatial resolution innermost layer [J. Baudot et al., IEEE-NSS 2009 conf. record]:



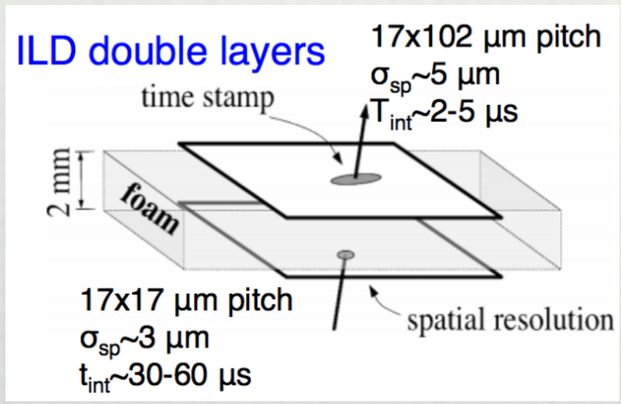
- reticle size detector, 0.35 µm OPTO
- on pixel correlated double sampling & ampli
- rolling shutter & parallel column readout



- binary output - 18.4 µm pitch
- sensor readout in 112 µs (80 MHz clock)
- σ = 3.5 µm
- fake hit rate 10^{-4} / pixel
- efficiency 99.5 +/- 0.1 %
- power consumption: 520 µW/column => 700 W for the full VD
- thinned down to 50 µm (et la PLUME!)

To turn RED into GREEN:

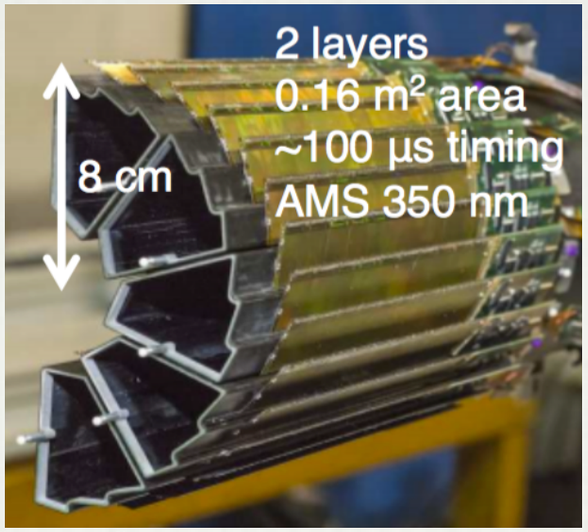
1.



2. explore smaller size feature, e.g. 180 nm (Tower-Jazz) + power pulsing (2% on)

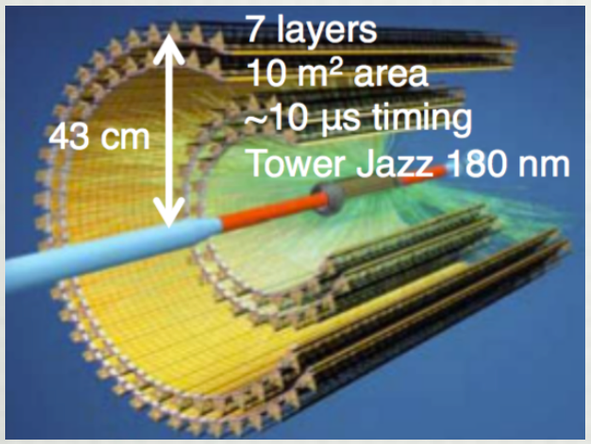
=> estimated to get to 15W consumption for the full VD

Another good point: the MAPS community commissioned already a large system for STAR:



- 400 sensors
- 0.9 Pixel each
- power dissipation 170 mW/cm^2

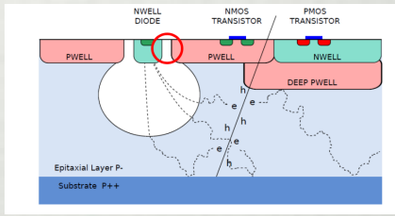
nothing but a toy compared to what is envisaged for the ITS of the ALICE experiment:



30 000 sensors

	σ_{sp}	$t_{r.o.}$	Dose	Fluency	T_{op}	Power	Active area
STAR-PXL	$< 4\ \mu m$	$< 200\ \mu s$	150 kRad	$3{\cdot}10^{12}$ n_{eq}/cm^2	30-35°C	160 mW/cm^2	0.15 m^2
ITS-in	$\lesssim 5\ \mu m$	$\lesssim$ **30** μs	**2.7 MRad**	**$1.7{\cdot}10^{13}$ n_{eq}/cm^2**	30°C	$<$ 300 mW/cm^2	0.17 m^2
ITS-out	$\lesssim 10\ \mu m$	$\lesssim$ **30** μs	100 kRad	$1{\cdot}10^{12}$ n_{eq}/cm^2	30°C	**$<$ 100 mW/cm^2**	**$\sim$ 10 m^2**

a development based on:



- new technologies (Tower-Jazz 180 nm)
- and new design (on pixel sparsification)

[P. Yang et al., Vertex 2014, JINST, doi:10.1088/1748-0221/10/03/C03030] ALPIDE
[G. Traversi, M. Caccia et al., IEEE-NSS conf record 2008] 130 nm STm Tech

DEPFET (DEPleted Field Effect Transistor)

[Kemmer & Lutz, NIM A253 (1987) 356]

Sideward depletion when

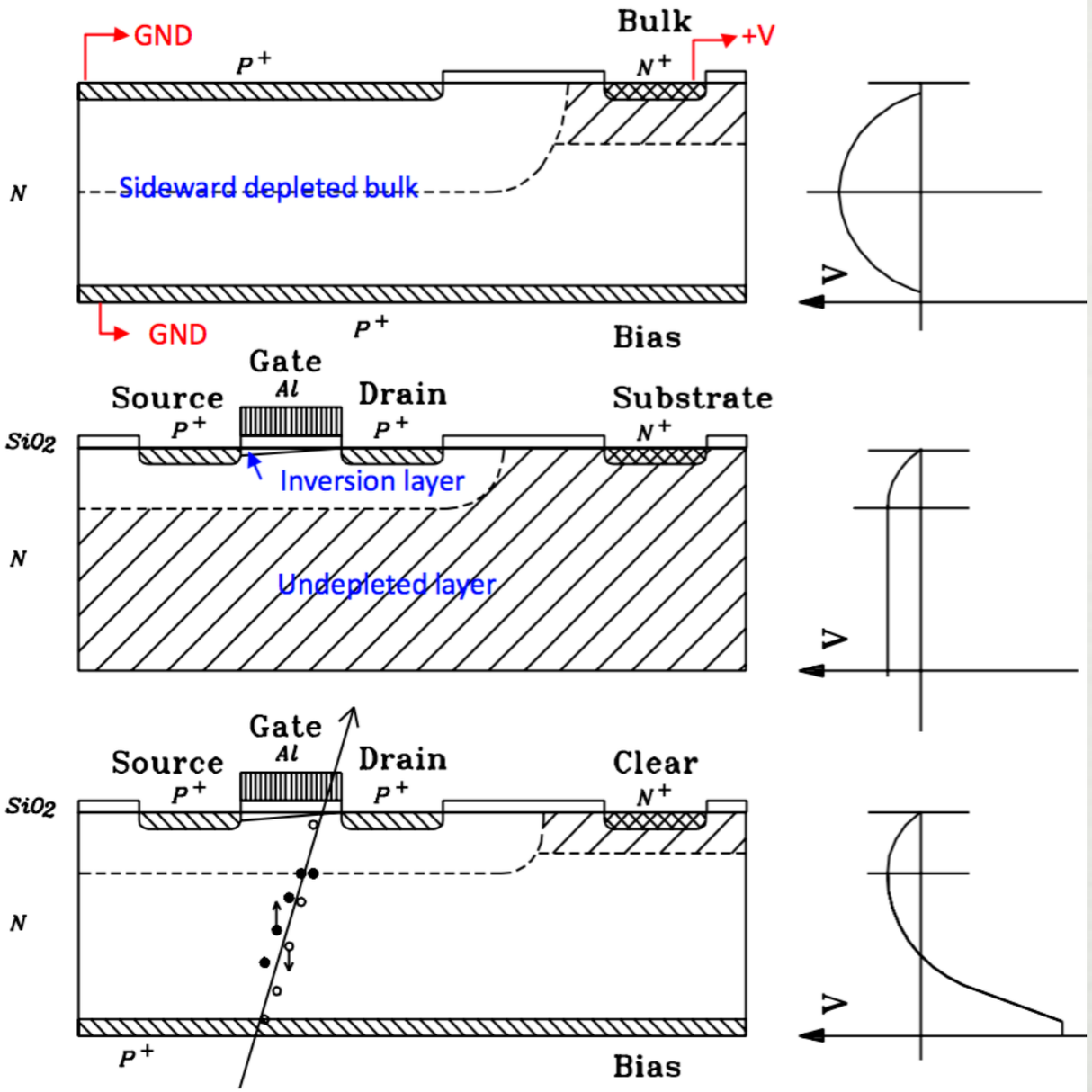
- diodes are located on both sides of a wafer
- substrate contact, located on the side, is polarized in the reverse bias direction with respect to the large-area diode junction
- A potential minimum for majority carriers (electrons in n-type silicon) forms between the two diode junctions.

MOS transistor

- A standard MOS enhancement-type transistor built on top of the bulk
- Conductivity of the channel steered not only by the gate voltage but also by the bulk potential.

DEPFET detector

- Bias applied on back side – minimum valley moves toward FET channel
- Holes moves toward back side
- Electrons toward the potential valley
- Mirrored charge in the FET gate open the channel and current flows.
- Positive signal applied to Clear electrode moves away electrons from valley and close the FET channel



internal gain 500 pA/e

© L.Rossi et al. [ref. b]

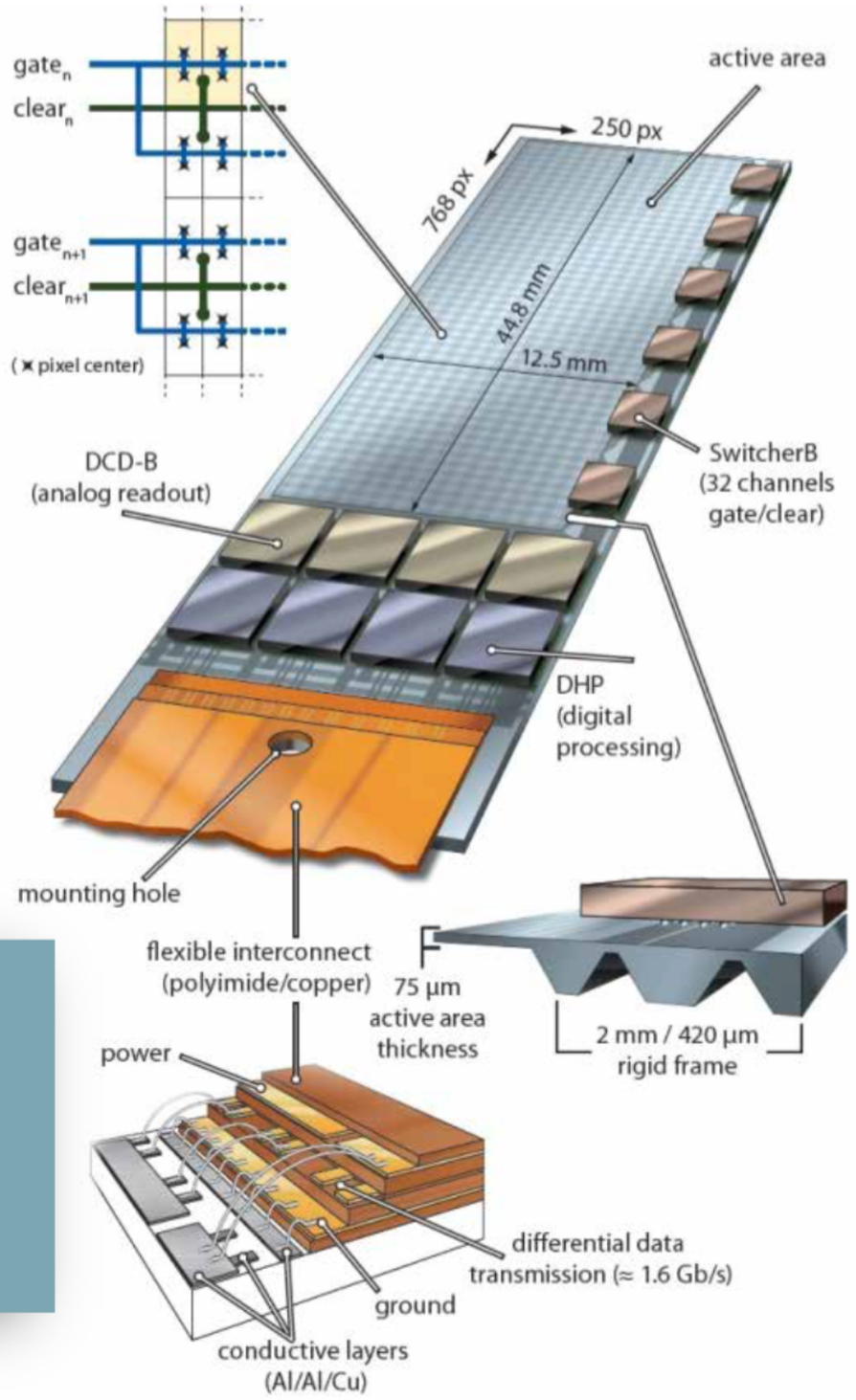
a. L.Rossi, T.Rohe, P.Fischer and N.Wermes, ***Pixel Detectors - From Fundamentals to Applications***. Springer, 2006.

DEPFET: an all-Silicon module (no CTE mismatch - but not exactly monolithic)

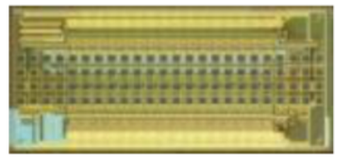
DCDB (Drain Current Digitizer)
Analog front-end

Amplification and digitization of DEPFET signals.

256 input channels
8-bit ADC per channel
92 ns sampling time
new version **w/ 50ns** sampling time under test
UMC 180 nm
Rad hard design

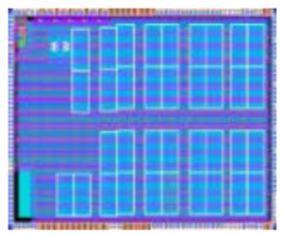


SwitcherB - Row Control



AMS/IBM HVCMOS 180 nm
Size 3.6 · 1.5 mm^2
Gate and Clear signal
32x2 channels
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

DHP (Data Handling Processor)
First data compression



TSMC 65 nm
Size 4.0 · 3.2 mm^2
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing and trigger control
Rad. Hard proved (100 Mrad)

Key to low mass vertex detectors

highest integration!
Thin sensor area
EOS for r/o ASICs
(perforated) silicon frame
w/ steering ASICs

L. Andricek, report at ALCW 2015 - JINST 10 C11002 (2015)

an All-Si module is a piece of art:

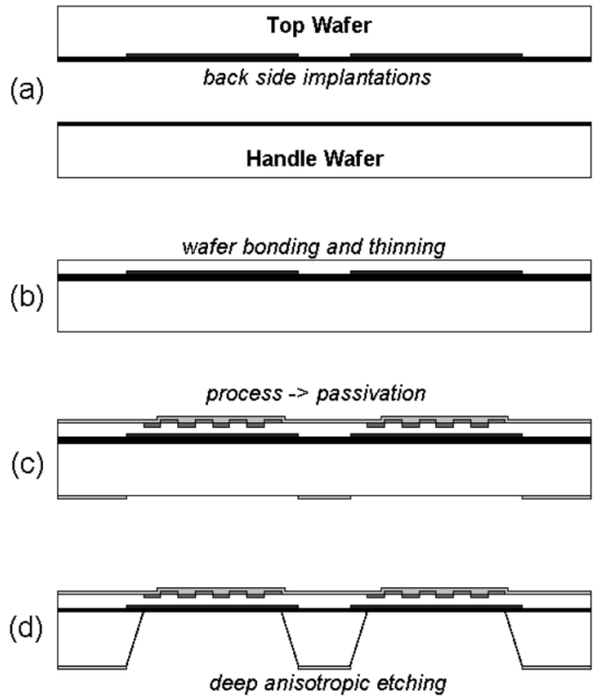
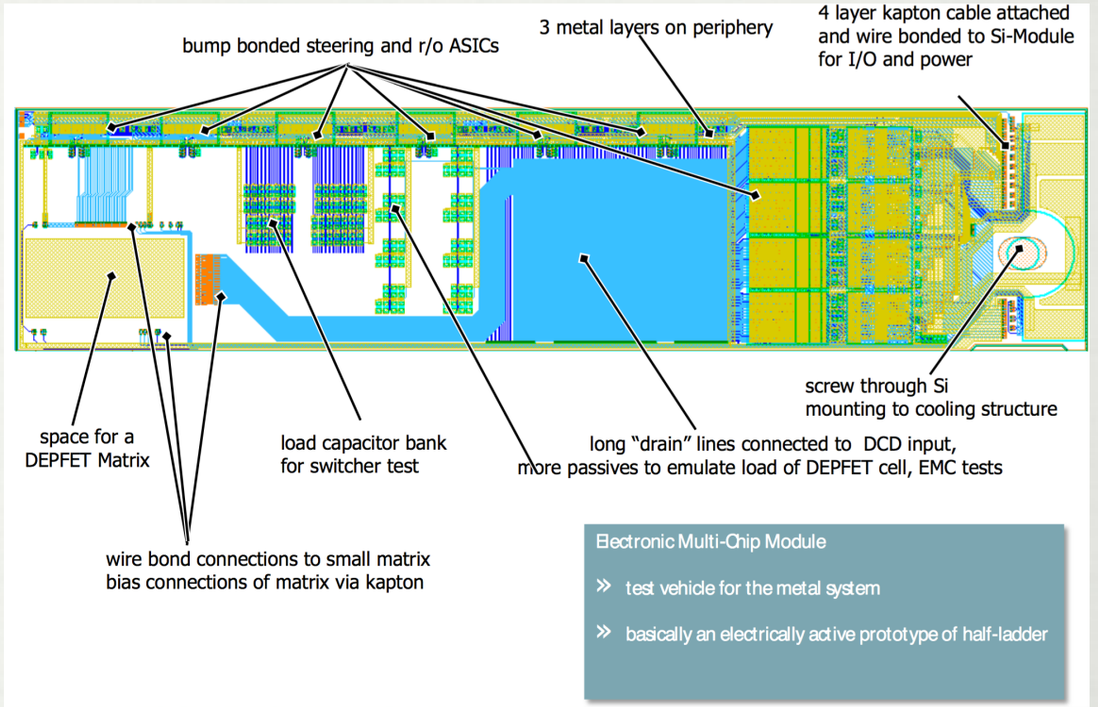


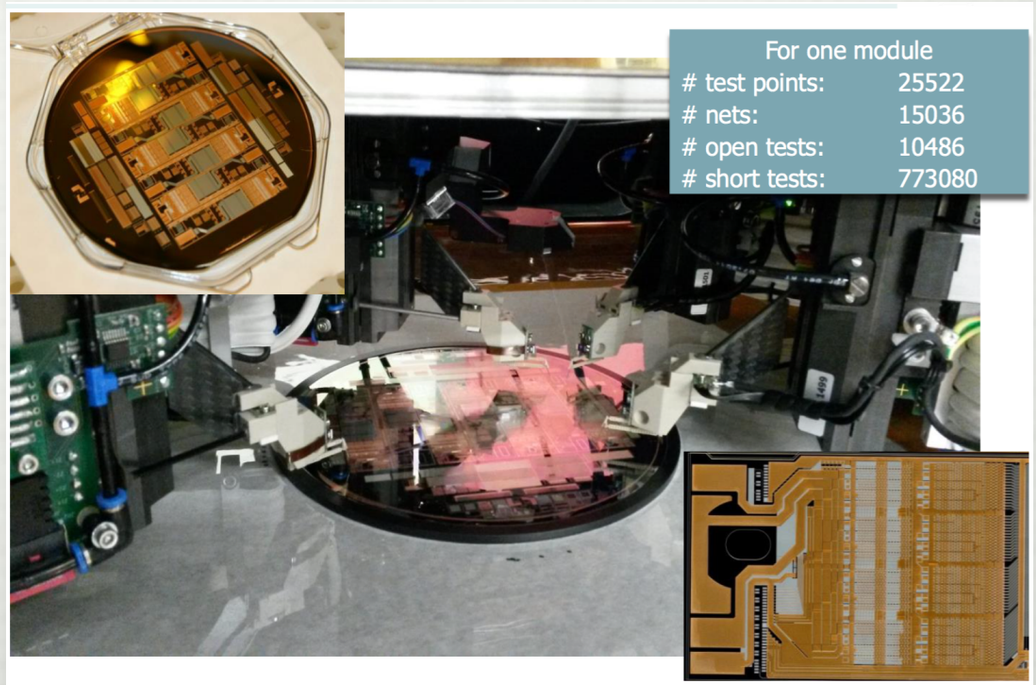
Figure 1: *Thinning of double sided processed detectors. a) The detector wafer, already after backside implantation, is bonded to a handle wafer. b) The detector wafer of the SOI stack is thinned. c) This stack can now be processed in a normal single sided production line. d) Finally the backside passivation of the handle wafer is removed at selected areas and the wafer etched away. The SiO_2 layer at the SOI interface acts as etch stop.*

HG. Moser et al PoS (Vertex2007) 013

and the frame is "active"

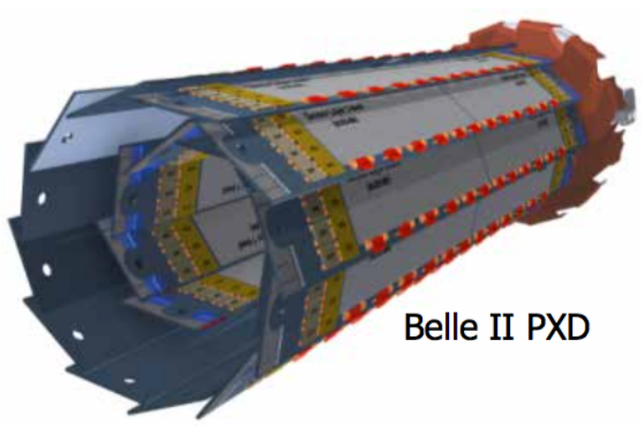


requiring extensive & sophisticated flying probe testing
JINST 10 C01049 (2015)

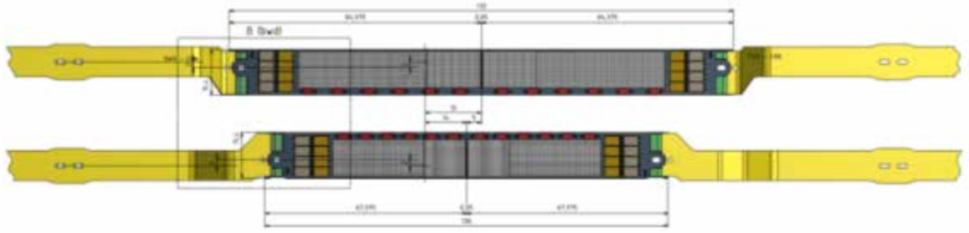


The DEPFET technology is also experiencing a very intense "stress test":

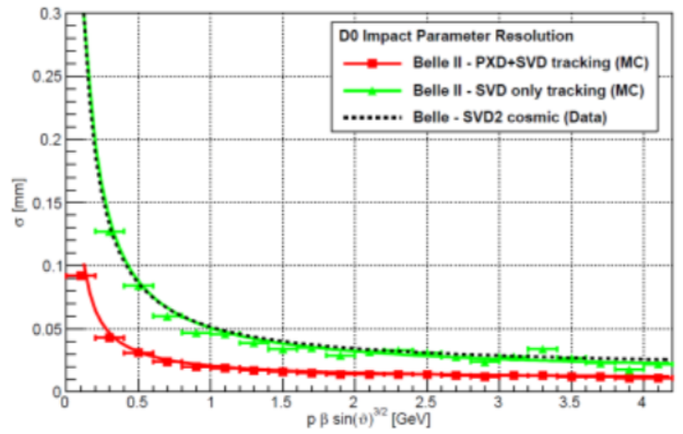
	ILD LOI 5-layer layout	Belle II	
Radii	15, 26, 38, 49, 60	14, 22	mm
Sensitive length	123 (L1), 250 (L2-L5)	90 (L1), 122 (L2)	mm
Sensitive width	13 (L1), 22 (L2-L5)	12.5 (L1-L2)	mm
Number of ladders	8, 8, 12, 16, 20	8, 12	
Pixel size	20x20 (L1-L5)	55x50 & 60X50 (L1), 70x50 & 85x50 (L2)	μm^2
r/o time per row	50 (L1), 250 (L2-L5)	100	ns
Number of pixels	800	8	Mpix



Belle II PXD



Belle II PXD ladder:
(almost) prototypes for L1 and L2 of ILD LOI layout!!



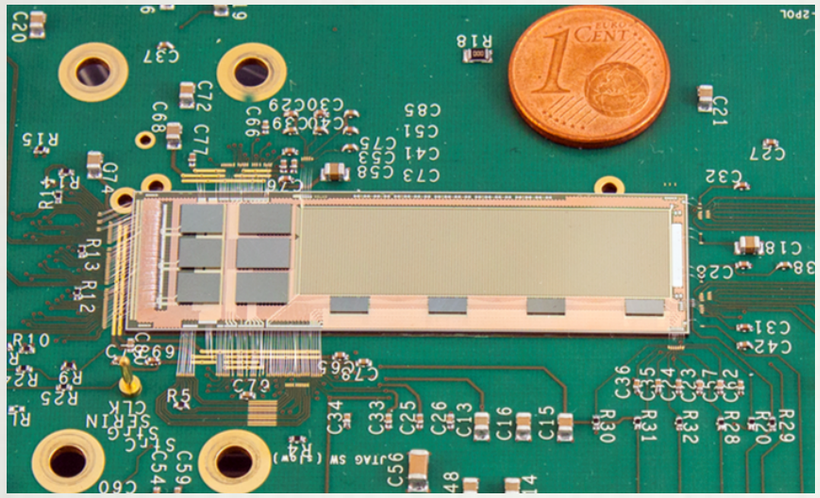
and the construction of the Belle II VD, irrespective from the non trivial differences, is certainly a valuable benchmark:

	Belle II pixel detector	ILD vertex detector
Occupancy [hits/μm^2/s]	0.40	0.13
TID per year [Mrad]	2.0	< 0.1
NIEL per cm^2 and year [1 MeV n_{eq}]	2.0×10^{12}	1.0×10^{11}
Frame readout time [μs]	20	25–100
Material budget per layer [X_0]	0.21 %	0.12%
Pixel pitch [μm^2]	50×75	20×20
Resolution [μm]	15	5

State of the art:

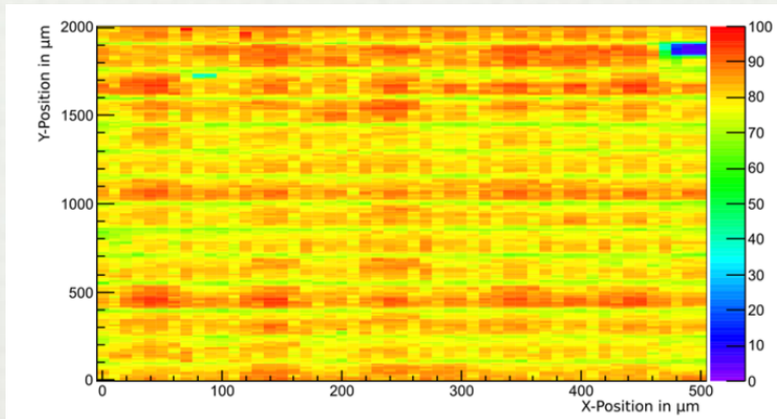
JINST 10 C11002 (2015)

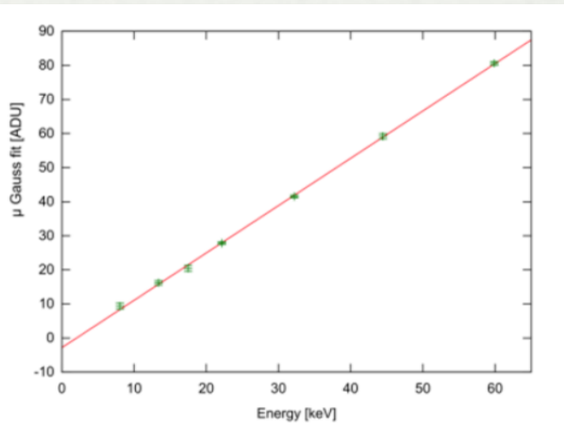
* full scale modules produced in 2014:



- 192 x 480 pixels, 50 x 75 μm^2 pitch
- 50 μm thin active area
- equipped with the final version of the Read-Out ASIC

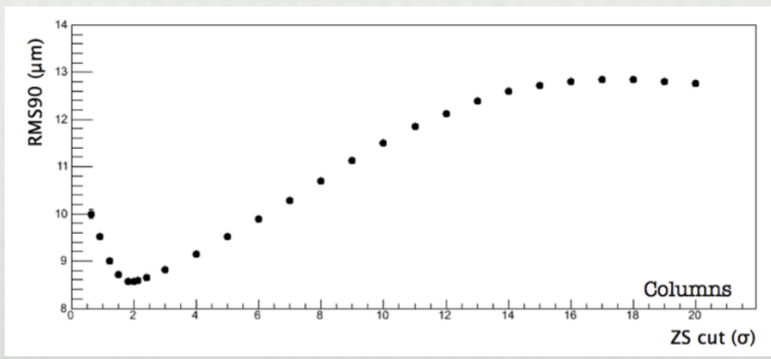
* charge collection uniformity & linearity assessed (lab test with a laser spot):





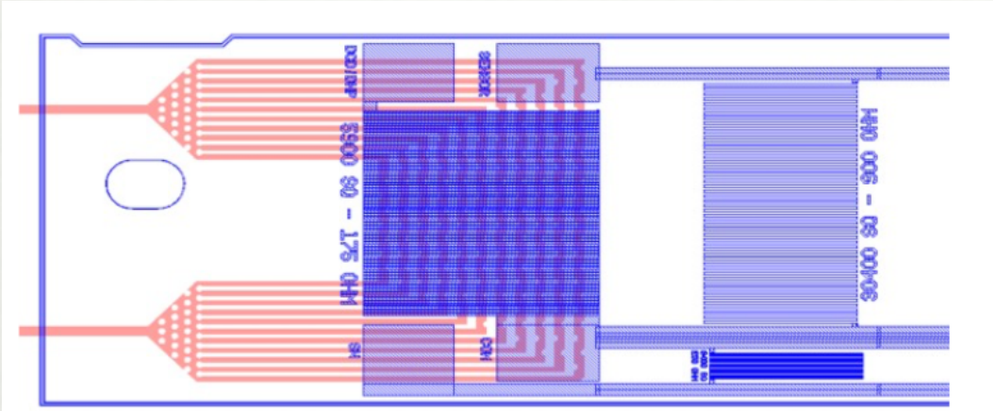
* ε = 99.5%, S/N = 40 and resolution = 8.5 μm:

resolution vs zero suppression cut

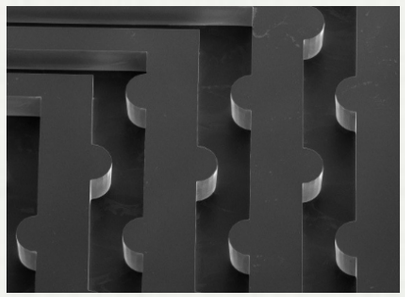


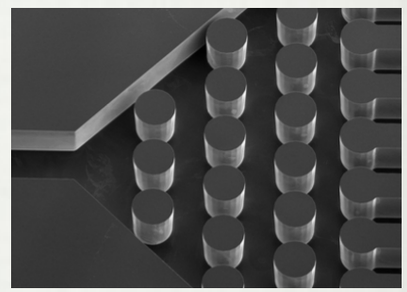
A note about power dissipation:

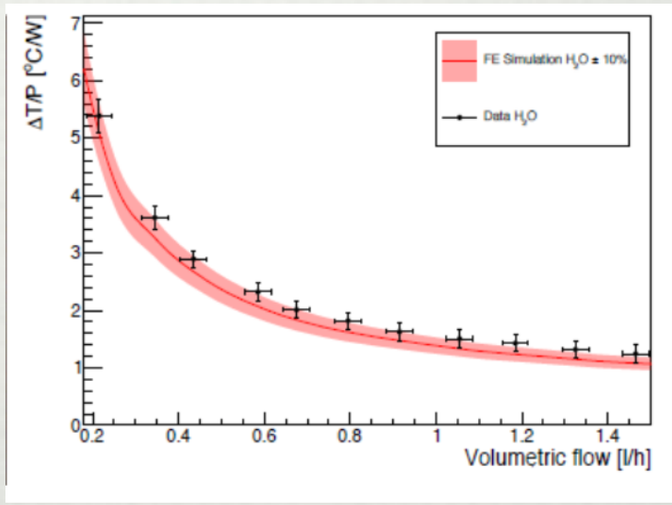
- the full BELLE VD is going to dissipate 9W
- for the ILD VD, integration is being pushed to the limit: process a pattern of cooling channels in the handle wafer of the SOI assembly (before bonding):



M. Vos, report at LCWS2015

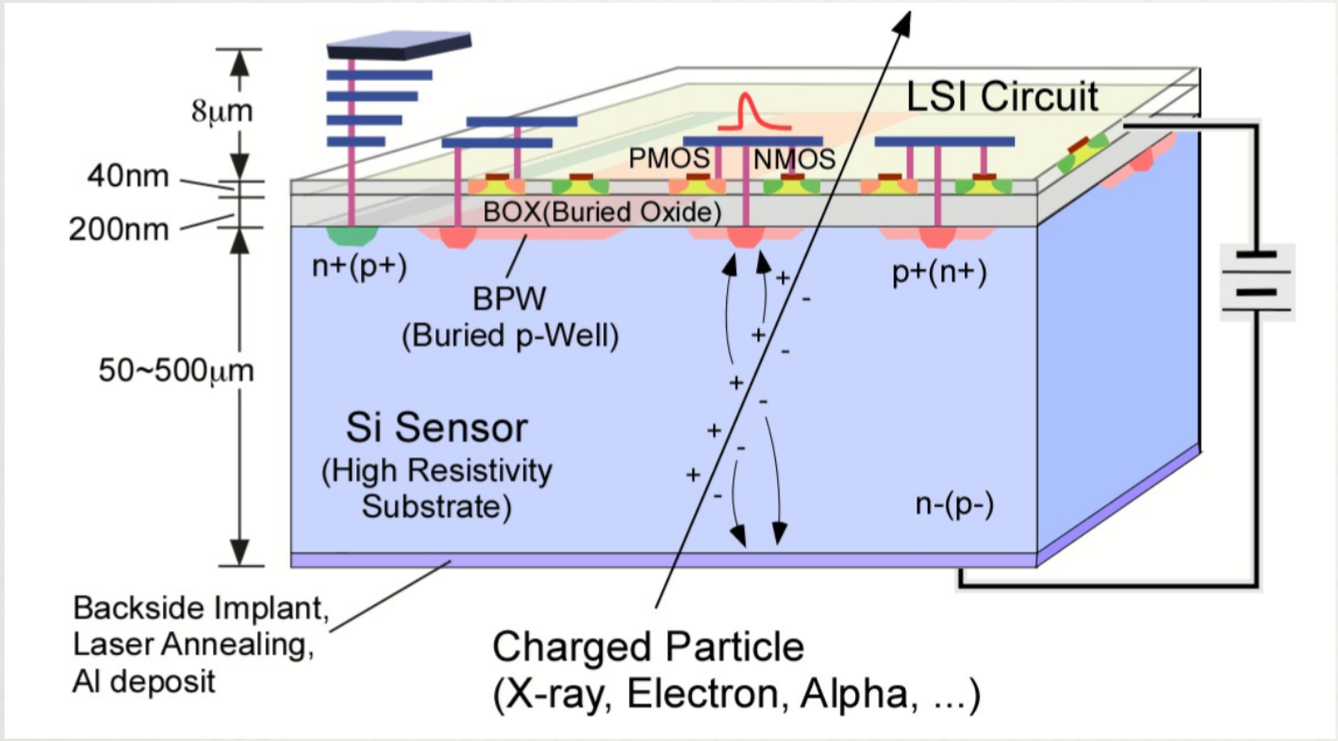


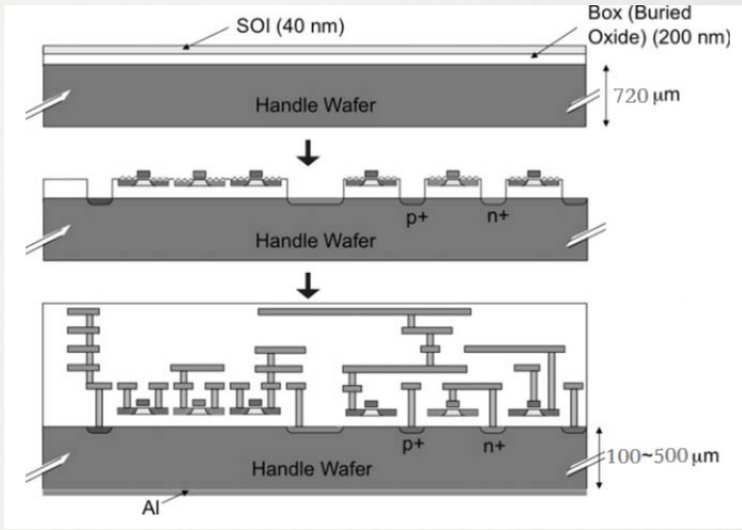




SOI pixels on high resistivity substrate

- H. Lan et al. IEEE sensors journals 15 (2015) 2732 a Review!
- J. Marczewski, M. Caccia et al., *IEEE Trans. Nucl. Sci.*, 51 (2004)1025
- M. Jastrzab, M. Caccia et al, NIM A560 (2006) 31

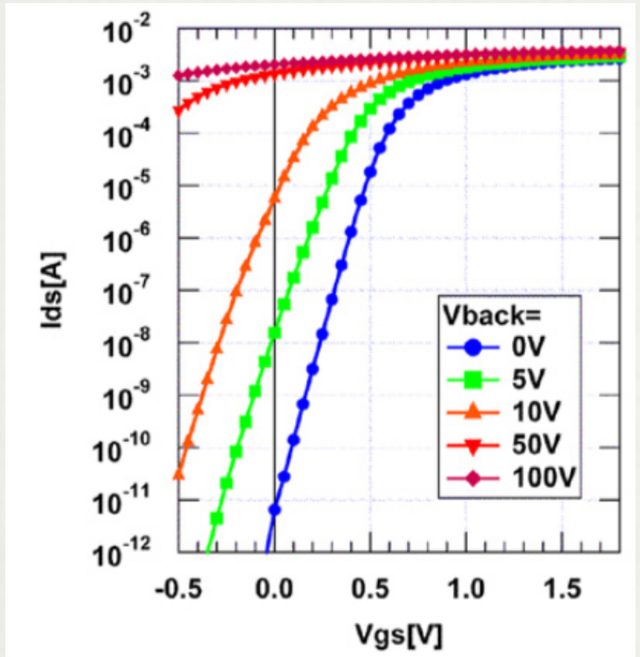




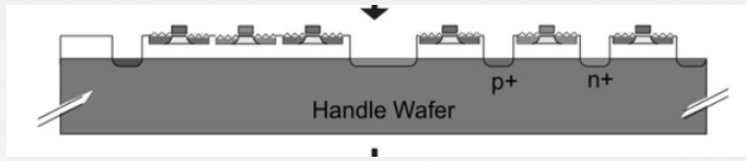
simplified process flow

- main advantages:
  - a genuine monolithic approach
  - more flexible wrt CMOS maps (nmos & pmos naturally integrated in the SOI layer)
  - electronics "isolated" from the bulk (fast switching, reduced single event upset) [the motivation for the industrial development of SOI - partially true here]
  - the active layer is a very standard and comfortable high resistivity, fully depleted detector
- main disadvantages:
  - not easy to get SOI wafers on a high resistivity substrate
  - mind the effect of the depletion voltage (back-gate effect)
  - custom process

A note on the back-gate effect:

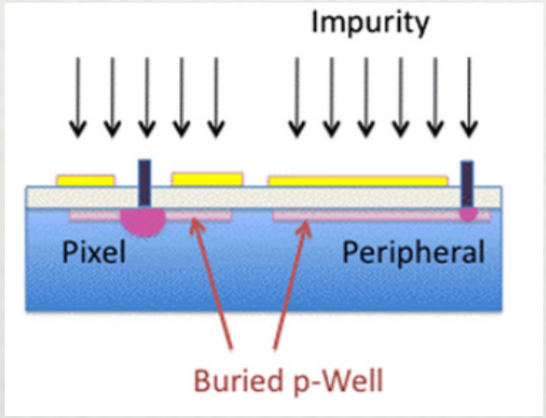


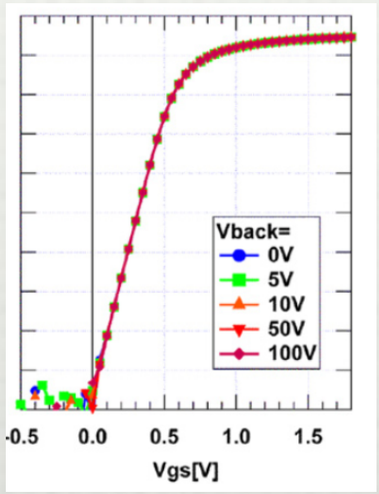
- the area under the transistor acts as a back gate: its potential affects the threshold voltage and the leakage current of the transistor



- The back gate effect is small compared to the front gate since the front gate oxide (4 nm) is much thinner compared with that of the buried oxide (200 nm).
- However, since the depletion voltage is O(100V), unfortunately the effect is quite visible

In order to overcome this problem, p-type dopants are implanted through the top Si layer and create a buried p-well (BPW) region under the BOX:

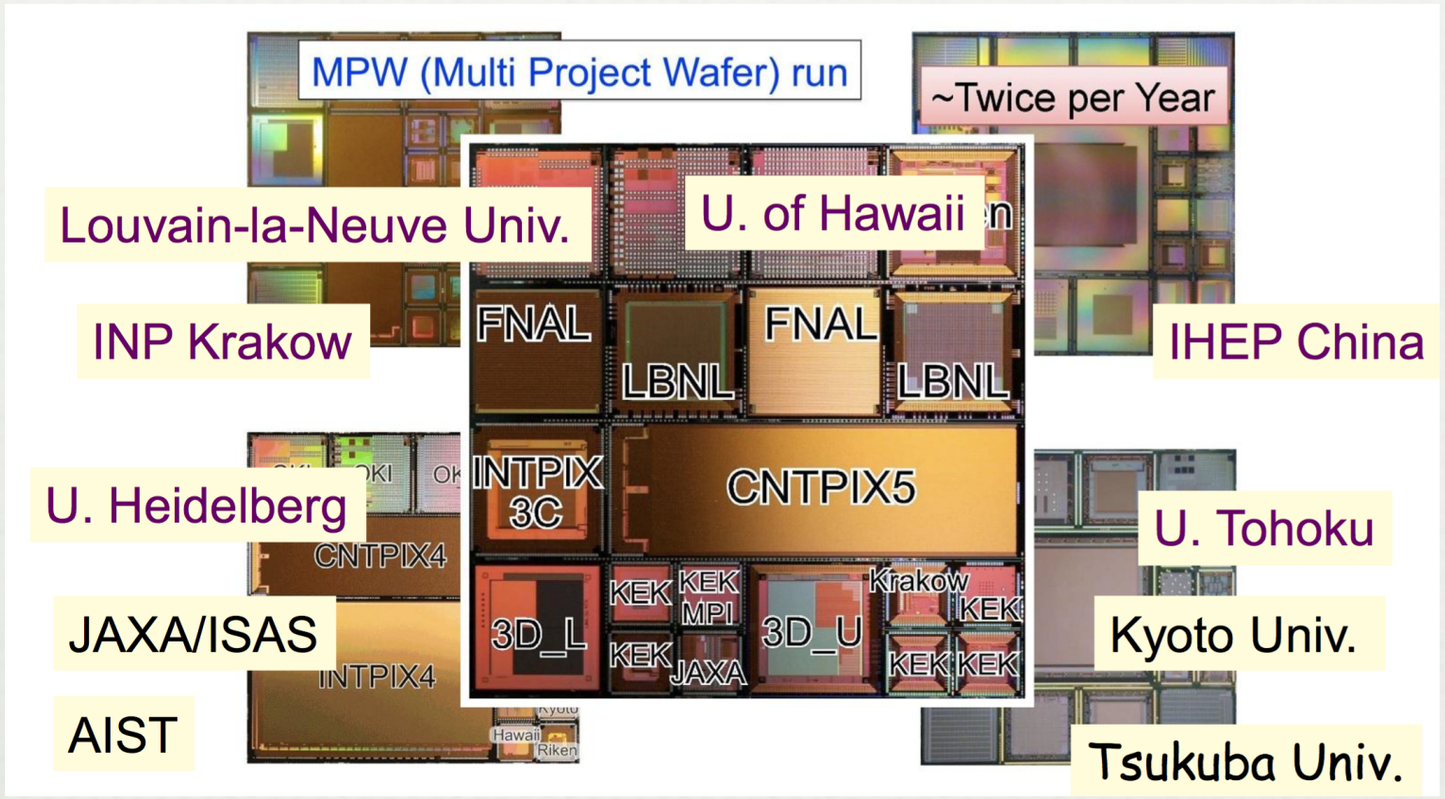




Y. Arai et al., NIMA 636 (2011) s31

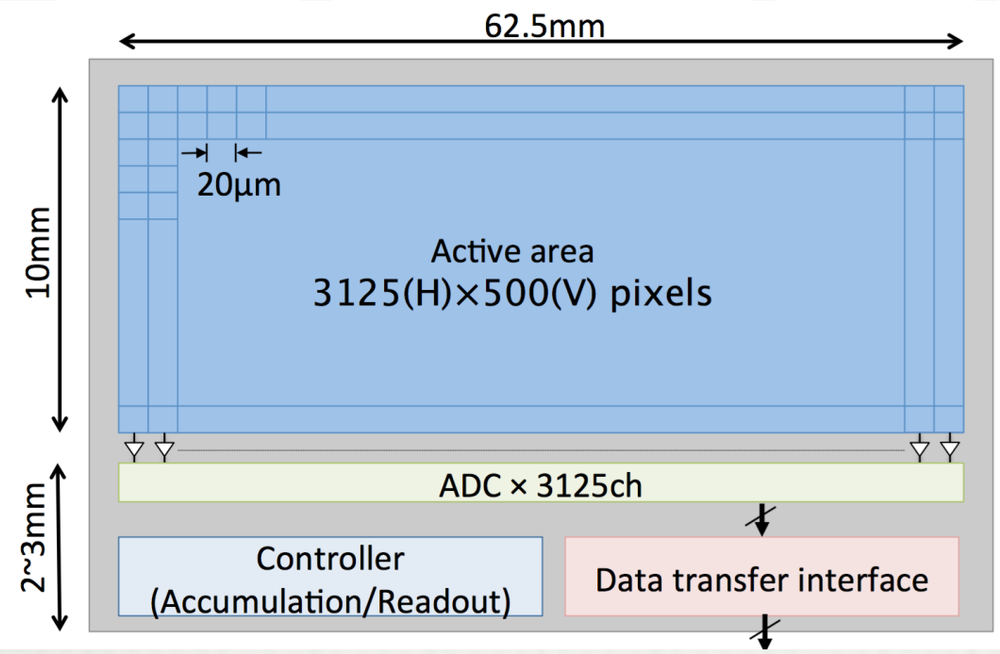
State of the art:

- there's a very active international collaboration, lead by KEK, exploring the 200 nm LAPIS technology (formerly OKI):

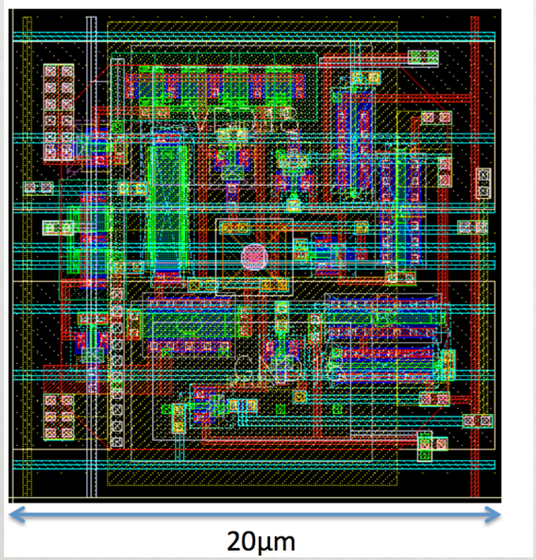


- several prototypes have been produced and characterised; the first ILC oriented prototype has been designed (SOFIST):

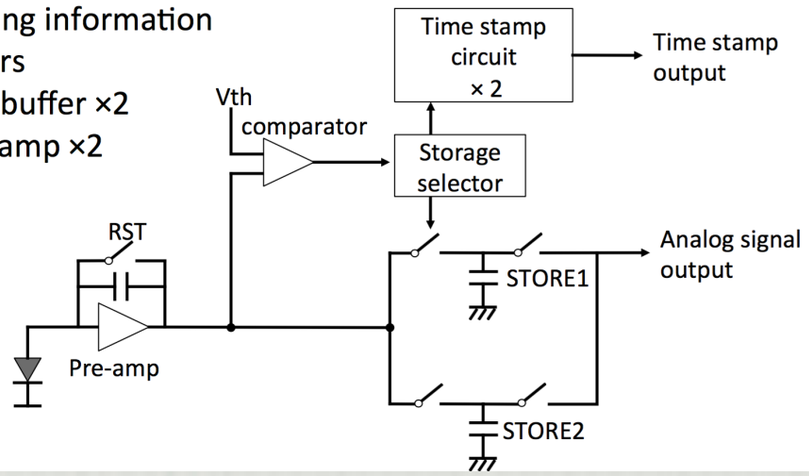
- SOI sensor for Fine measurement of Space and Time



- delivery expected Nov. 2015
- characterisation & prototype 2 in 2016



- Storage
  - Charge signal generated by particle
  - Hit-timing information
- Multi buffers
  - Analog buffer ×2
  - Time stamp ×2



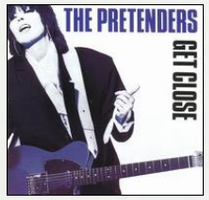
Conclusions:

Can we be:

- PRECISE

- SLIM

- "CLOSE"



- SHARP

- FAST
- AND KEEP COOL AT THE SAME TIME?


YES WE CAN