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Vertex and silicon tracking system of CEPC detector

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On behalf of the CEPC Vertex detector sub-group

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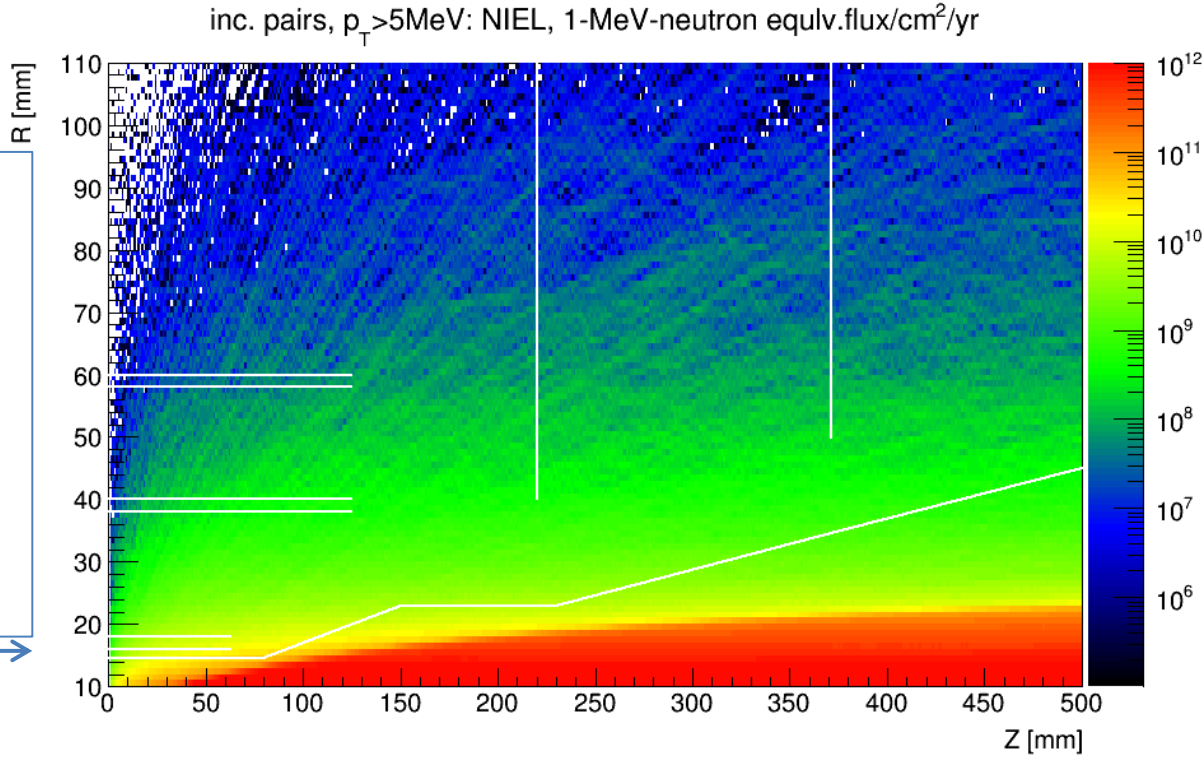
Outline

- *Detector requirements*
- *Detector concept*
- *Performance optimization*
- *Technology options*
- *Critical R&D*
- *Summary / Conclusions*

Backgrounds in inner tracking region

The NIEL (Non-Ionising Energy Loss) distribution introduced by the particles originating from the beam-beam interactions.

The averaged hit density ~0.2/cm^2/BX
→ detector occupancy <0.5%
for the innermost vertex detector layer.



Detector requirements

B=3.5T

Efficient tagging of heavy quarks

- momentum resolution $\sigma_{1/p_T} = 2\times10^{-5} \oplus 1\times10^{-3} /(p_T \sin\theta)$
- impact parameter resolution $\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\,\mu m$

Vertex detector specifications:

- σ_{SP} near the IP: *≤3 μm*
  → small pixels 16×16μm² or below, digital readout
- material budget: *≤ 0.15%X $_0$/layer*
  → low power circuits, air cooling
- pixel occupancy: *≤ 0.5 %*
- radiation tolerance: Ionizing dose *≤100 kRad/ year*
  Non-ionizing fluence *≤$10^{11} n_{eq}$/ (cm^2 year)*
- first layer located at a radius: *~1.6 cm*

Silicon tracker specifications:

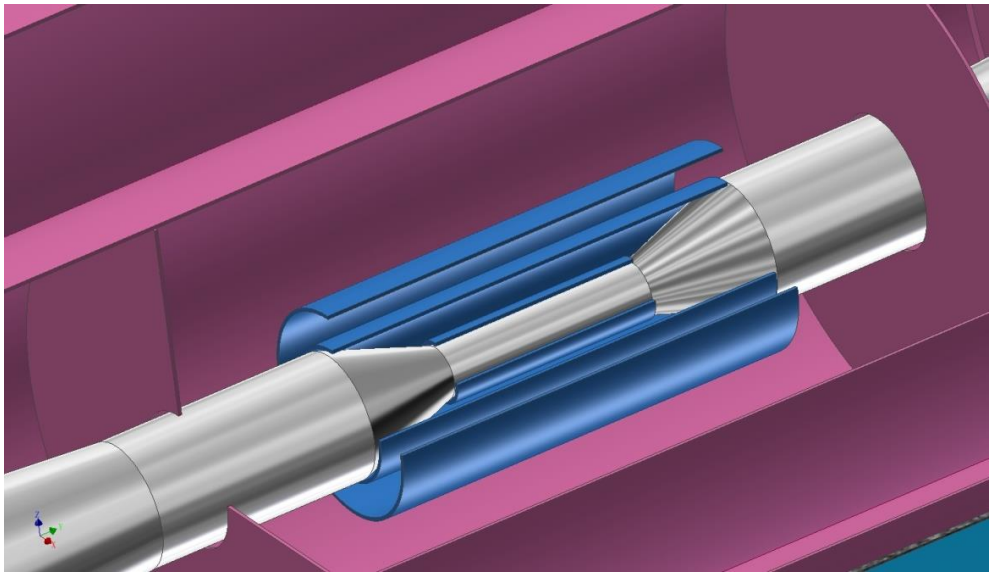
- σ_{SP} : *≤ 7 μm* → small pitch (50 μm)
- material budget: *≤ 0.65%X $_0$/layer*

Detector concept

ILD-like but different forward region design

Vertex detector：

- 3 double-sided pixel layers
- σ_{SP}=2.8 μm, inner most layer
- readout time <20 μs

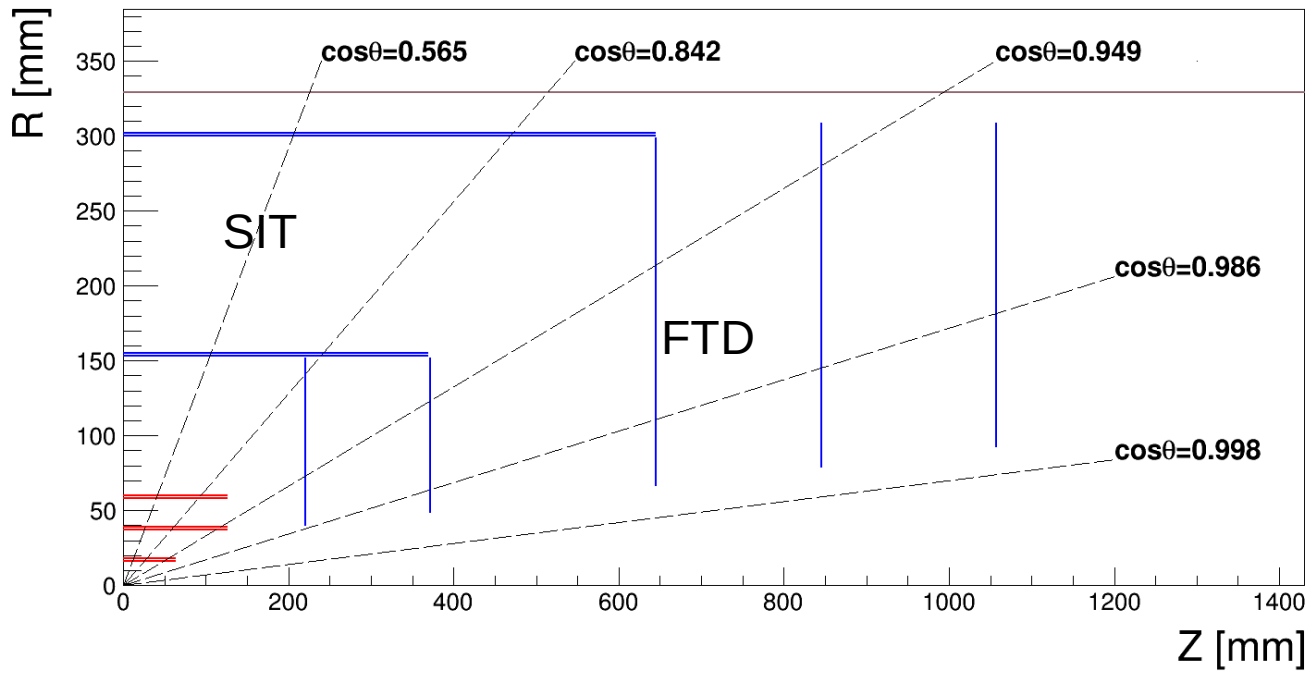


Vertex detector parameters

	R (mm)	|z| (mm)	$\|\cos\theta\|$	σ_{SP} (μm)	Readout time (μs)
Layer 1	16	62.5	0.97	2.8	20
Layer 2	18	62.5	0.96	2.8	20
Layer 3	37	125.0	0.96	4	20
Layer 4	39	125.0	0.95	4	20
Layer 5	58	125.0	0.91	4	20
Layer 6	60	125.0	0.90	4	20

Detector concept (Cont.)

Si-tracker : SET and ETD not shown



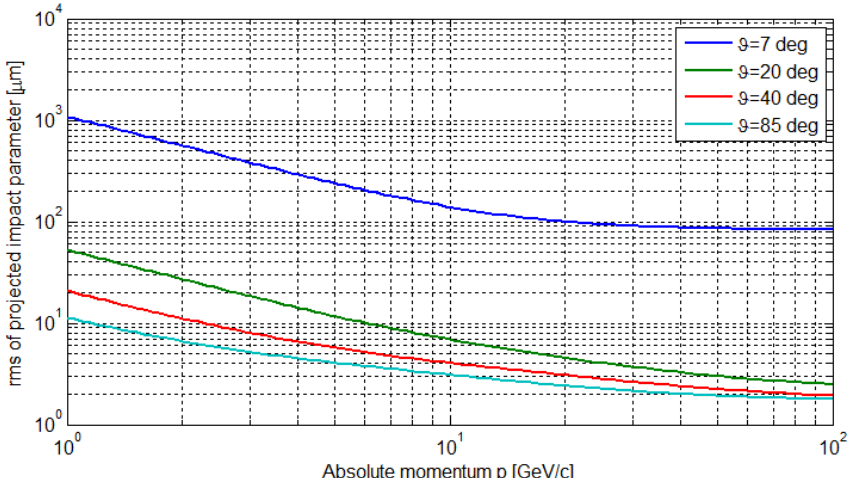
- Silicon Internal Tracker (SIT) – 2 inner layers Si strip detectors
- Forward Tracking Detector (FTD) – 5 disks (2 with pixels/3 with Si strip sensor) on each side (7 disks for ILD) due to the smaller L*
- Silicon External Tracker (SET) – 1 outer layer Si strip detector
- End-cap Tracking Detector (ETD) – 1 end-cap Si strip detector

Performance optimization

LDT: fast simulation using the **Kalman Fitter**

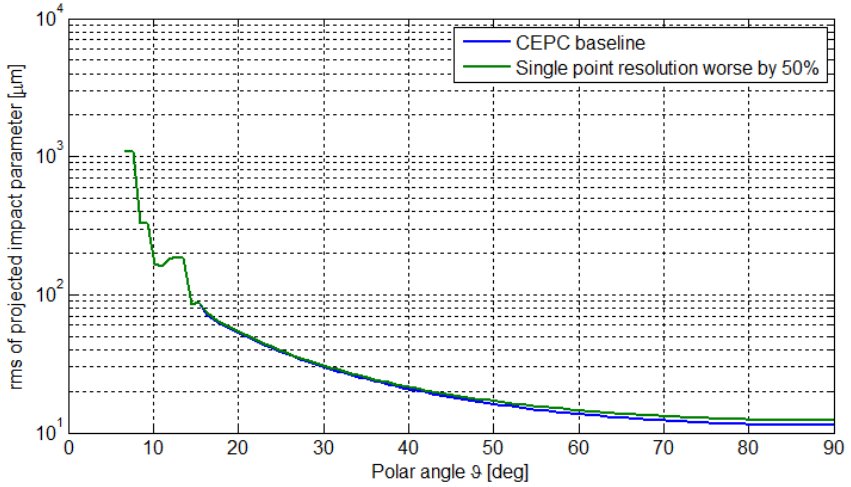
Baseline design performance

Resolutions of the transverse impact parameter for single muons



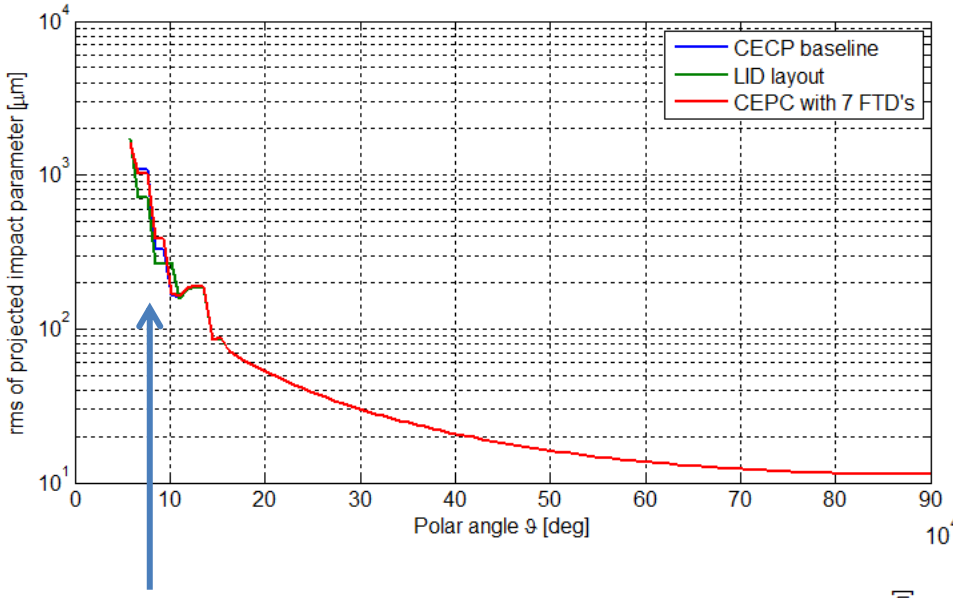
Single point resolution

Transverse impact parameter resolution as a function of the polar angle for different values of the single point resolution of the pixel sensors



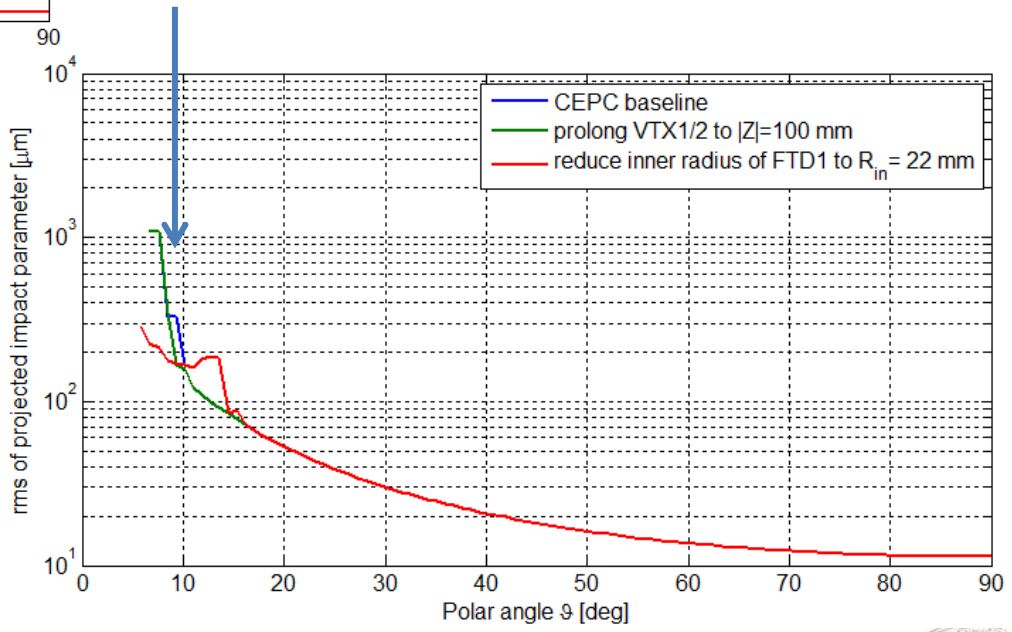
Performance optimization (Cont.)

- Configurations of the forward layout for L*=1.5m



Performance loss in the low polar angle region (impact parameter resolution of tracks) with reduced number of FTD disks

The performance loss can be recovered with extended coverage of the pixel detector layers, either by prolonging first two VTX barrel layers or extending the first FTD disk down to r=22mm



Technology options

Many technologies from ILC/CLIC could be referred to. BUT, unlike the ILD, the CEPC detector will operate in continuous mode.

Pixel sensor: power consumption < 50mW/cm^2 , if air cooling used, readout time < 20 μs

- HR-CMOS sensor with novel readout structure – ALPIDE for the ALICE ITS Upgrade
  - relatively matured technology
  - <50 mW/cm^2 expected
  - Capable of readout every ~4μs
- SOI sensor with similar readout structure
  - Fully depleted HR substrate, potential of 15μm pixel size design
  - Full CMOS circuit
- DEPFET: possible application for inner most vertex layer
  - small material budget, low power consumption in sensitive area

Silicon microstrip sensor: p$^+$-on-n technology, or pixelated strip sensors based on CMOS technologies

Critical R&D

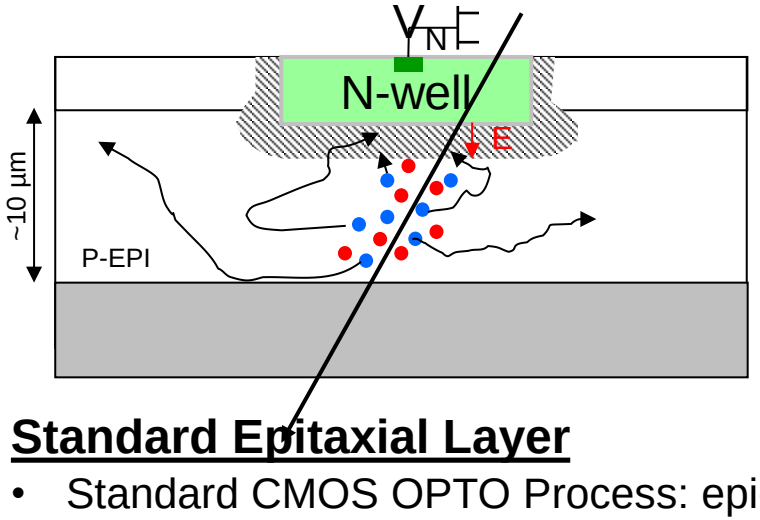
- Sensors with low power consumption and high readout speed

  In-pixel discriminator
  In-matrix sparsification

  } Similar to the ALPIDE sensor for the ALICE ITS Upgrade

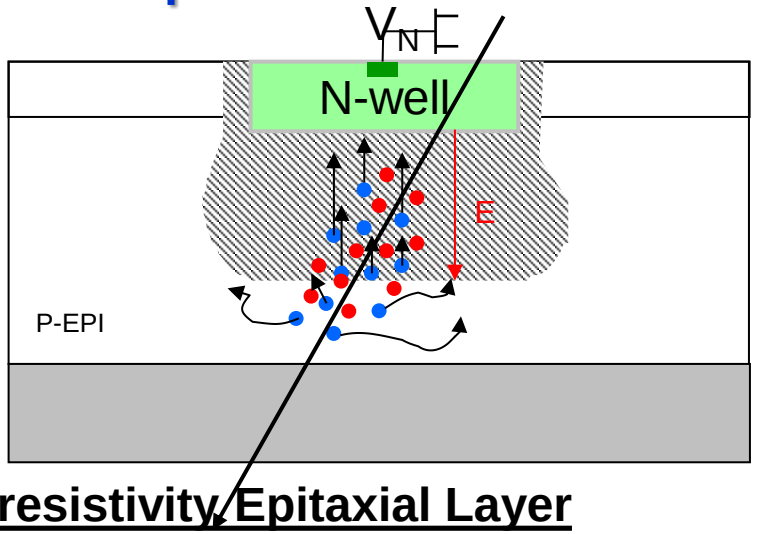
  - Starting design with HR-CMOS process
  - Exploring possibility with SOI process, especially small pixel size
- Light weight mechanical design and cooling
  - 0.05%(0.1%) material budget without/with cabling
  - Air cooling technology with acceptable vibration due to air flow
- Thinning pixel sensor down to 50μm
- Slim-edged silicon microstrip sensors
- Low noise and low power consumption front-end electronics for silicon microstrip

Critical R&D: HR-CMOS pixel sensor



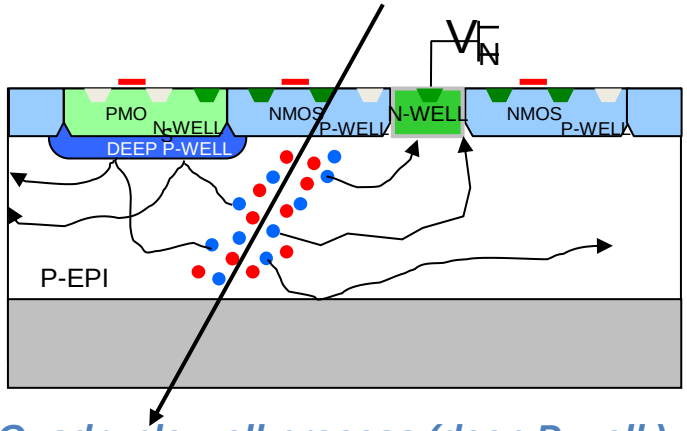
Standard Epitaxial Layer

- Standard CMOS OPTO Process: epi-layer resistivity ~10 Ω*cm
- Charge collection: thermal diffusion
- Collection time: O(100 ns)



High resistivity Epitaxial Layer

- Higher resistivity >1 kΩ*cm & thicker (~40 µm) epi-layer
- Charge collection: drift/thermal diffusion
- Collection time faster, less recombination ➔ radiation tolerant
- Depletion depth depends on bias



Quadruple well process (deep P-well): 0.18 µm

ALICE ITS upgrade: 2 sensors R&D using the TowerJazz CIS 0.18 µm process

- Synchronous Readout R&D
- Asynchronous Readout R&D

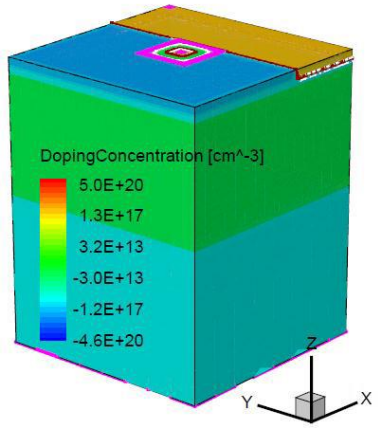
Courtesy of Christine Hu-Guo, IPHC-Strasbourg

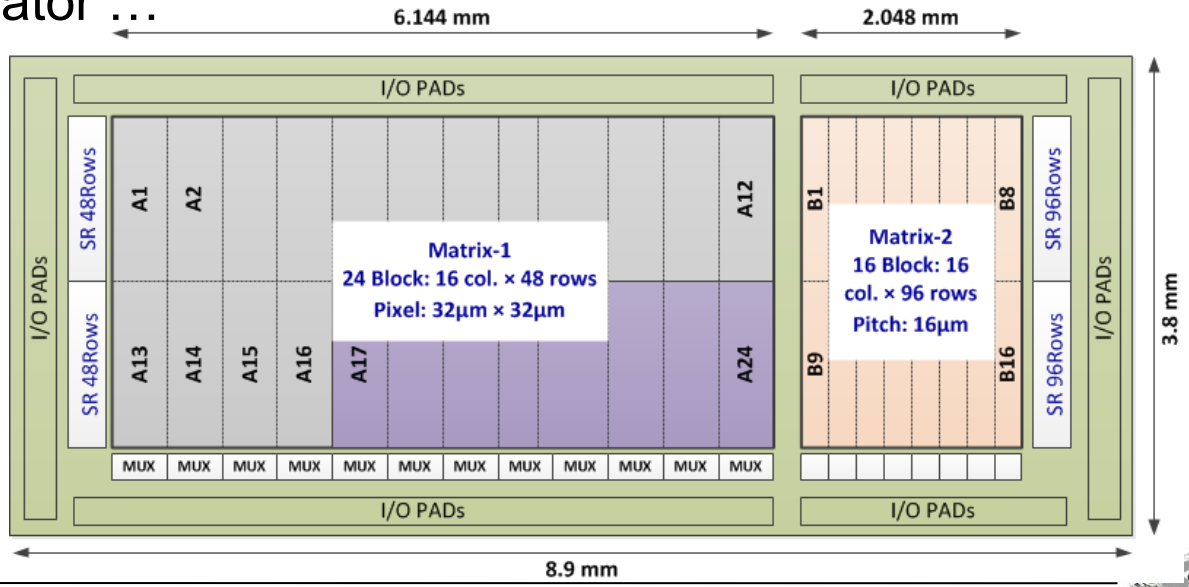
Critical R&D: HR-CMOS pixel sensor (Cont.)

First Step: sensor diode optimization (charge collection efficiency/time) with TCAD simulation and *to be verified with sensor characterization*

First submission expected in June 2015

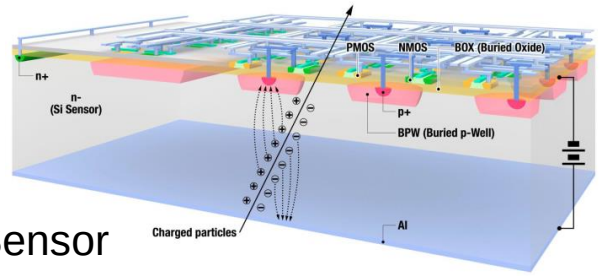
- Pixel sizes of 32 × 32 um^2 (A1-16) and 16 × 16 um^2 (B1-16), with different configurations (set of parameters) of sensor diode, 2/3T structure, read out with rolling shutter
- A17-24 verification of in-pixel electronics (analogue only), e.g. current comparator, discriminator …





Critical R&D: Readout Scheme Based on SOI technology

- Fully CMOS pixel circuit
  - Low power and compact layout
- Large mask size and regular MPW run
  - 35mm * 25mm
  - Twice/year since 2009
- Detector-oriented process
  - HR wafer, BPW, Double SOI…
- Signal charge increased by a factor of 4
  - 4000e$^-$ vs 1000e$^-$

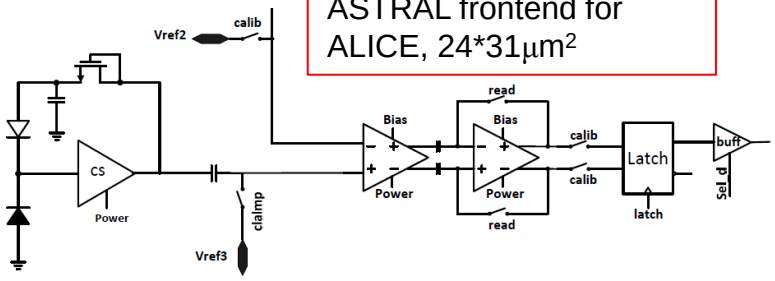


SOI Sensor

	SOI	HR-CMOS
Process	0.2μm CMOS	0.18μm CMOS
Mask Size	35mm*25mm	32mm*25mm
Sensitive	50μm bulk	15μm epitaxial
Depletion	Fully	Partially
Charge Collection	Drift	Diffusion
Signal Charge	~4000e$^-$	~1000e$^-$

- Pixel size ~16um
  - To achieve 3μm point resolution
- In pixel discriminator
  - Reduce the driven current in case of column discriminator
- Develop in-pixel circuit for minimum layout area with a profitable 4 times larger signal charge.

ASTRAL frontend for ALICE, 24*31μm^2



Summary/Conclusions

- Baseline design for pre-CDR
- An ILD-like vertex and Si-tracker layout, with modifications in forward region
- Layout optimization studies using fast simulation
- Critical R&D underway
- New participation welcomed

Thanks for your attention!