

IEEE TRANSACTIONS ON ELECTRON DEVICES

# A Bottom-Gate Metal–Oxide Thin-Film Transistor With Self-Aligned Source/Drain Regions

Zhihe Xia<sup>®</sup>, Lei Lu<sup>®</sup>, *Member, IEEE*, Jiapeng Li<sup>®</sup>, Hoi-Sing Kwok, *Fellow, IEEE*, and Man Wong, *Senior Member, IEEE* 

Abstract — Proper driving of a large-area, high-resolution, and high-frame-rate active-matrix display can be hindered by excessive delay along a signal path, such as a scan line. Depending on the transistor architecture, such delay could be dominated by the parasitic overlap capacitance between the gate electrodes and the source/drain (S/D) regions of the address-transistors attached to a scan line. While the capacitance can be minimized by employing a transistor with the edges of the regions selfaligned (SA) to those of the electrode, actual implementation is easier with a top-gate rather than the more commonly deployed bottom-gate architecture. Presently reported is the realization and characterization of a bottomgate, SA indium-gallium-zinc oxide transistor. The extent of the overlap between the S/D and the gate is determined by a thermal "activation" process, similar to how it is controlled in a conventional top-gate, SA transistor.

Index Terms—Elevated-metal-metal-oxide (EMMO), indium-gallium-zinc oxide (IGZO), parasitic capacitance, *RC* delay, self-aligned (SA), thin-film transistor (TFT).

### I. INTRODUCTION

MATRIX display is commonly driven by sequentially addressing its rows of scan lines. The delay of a signal propagating along a scan line is determined largely by the product of the associated resistance (R) and capacitance (C), with a larger RC time-constant corresponding to longer delay. With increasing display size, resolution, and frame rate, R and C must be adjusted accordingly. The two main components making up C are the capacitance of the interconnect and that of the attached address transistors. The latter can be further decomposed to include an intrinsic gatechannel capacitance and a parasitic gate-source/drain (S/D) overlap capacitance.

Manuscript received March 23, 2018; revised April 26, 2018; accepted May 1, 2018. This work was supported by the Partner State Key Laboratory on Advanced Displays and Optoelectronics Technologies under Grant ITC-PSKL12EG02. The review of this paper was arranged by Editor X. Guo. (*Corresponding author: Man Wong.*)

Z. Xia, J. Li, and M. Wong are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: eemwong@ust.hk).

L. Lu and H.-S. Kwok are with the Department of Electronic and Computer Engineering and also with the HKUST Jockey Club Institute for Advanced Study, The Hong Kong University of Science and Technology, Hong Kong.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2018.2833057

The bottom-gate, staggered thin-film transistor (TFT) architecture is commonly used [1], [2] in a matrix display. An inevitable overlap exists between the gate electrode and the S/D regions or electrodes of a TFT, due to the requirement of finite-alignment margins. The resulting parasitic overlap capacitance [3], [4] contributes to larger *RC*. Such parasitic capacitance, hence also its undesirable effects, can be reduced by employing a TFT with the edges (junctions) of the S/D regions self-aligned (SA) to those of the gate electrode. It is for this reason that top-gate, SA TFT, an architecture not commonly used in large-area matrix displays, was deployed in recently commercialized large size (>65 in), ultrahigh definition (such as 8K), and high frame-rate (>120 Hz) television sets [5].

Attributed to their compatible fabrication process with the incumbent amorphous silicon TFTs and their relatively higher field-effect mobility ( $\mu_{\text{FE}}$ ), metal–oxide (MO) TFTs [6]–[8] such as those based on indium–gallium–zinc oxide (IGZO) are being deployed in the back planes of a new generation of active-matrix displays [9]–[12]. Recently, SA MO TFT structures have also been investigated [13]–[18], addressing the issues of parasitic capacitance.

MO can be made conductive by reaction with aluminum [13], plasma [14] or wet etching treatment [15], ion implantation [16], deep ultraviolet irradiation [17], laser annealing [18], hydrogen doping [19], or nonoxidizing thermal annealing [20]. When applied to a top-gate architecture, some of these techniques could be used to realize an SA TFT. However, common gate-electrode materials such as copper (Cu) and molybdenum (Mo) are gas-impermeable. Since defects are generated rather than annihilated in a transistor channel during a thermal treatment subsequent to the formation of the impermeable gate electrode [21], it has been pointed out [5] that a top-gate MO TFT exhibits poorer performance and reliability than a bottom-gate TFT-particularly if the latter is protected by an etch-stop (ES) layer and incorporates a fully oxidized channel. To maintain process continuity and to obtain better TFT reliability, one would desire a technology enabling selfalignment of the junctions with a bottom-gate architecture. Though self-aligned, bottom-gate structures based on a back-side exposure process have been proposed [18], [22]; these methods incur a penalty in terms of process complexity (hence cost) because the channel and the S/D regions are separately formed.



Fig. 1. (a) Scan line modeled as a distributed *RC* network in a display panel. (b) Layout of a subpixel.

In this paper, *RC* of matrix displays employing different TFT architectures is compared. The contribution of the parasitic overlap capacitance is made apparent. Based on the distinct effects of oxidizing thermal annealing on the properties of MO semiconducting thin films under covers of different gas-permeabilities [23], the elevated-metal metal–oxide (EMMO) TFT architecture has been proposed and demonstrated [24], [25]. A distinguishing feature of the EMMO architecture is the self-alignment of the thermally induced S/D regions to a gas-impermeable cover layer. Presently this feature is exploited to realize an SA, bottom-gate TFT with a fully oxidized channel region. The effects of the thermal treatment on the location of the induced S/D junctions were first investigated. This was followed by the fabrication and characterization of EMMO TFTs with SA S/D junctions.

## II. ANALYSIS OF RC DELAY OF A SCAN LINE

For a display of respective horizontal and vertical dimensions of  $S_{\rm H}$  and  $S_{\rm V}$ , the present analysis is based on the assumption of a "square" pixel of pitch *P* and a technology with minimum lithography resolution of  $\lambda$ . Shown in Fig. 1(a) and (b) are the respective schematics of a scan line modeled as a distributed resistor-capacitor network and the layout of a subpixel. Defined as the time taken to reach 90% of the strength of a signal under transmission, the time constant  $T_{RC}$  of the scan line is given approximately by [26]

$$T_{RC} \approx 3N_{\rm H}R_{\rm PX} \times 3N_{\rm H}C_{\rm PX} = 9N_{\rm H}^2R_{\rm PX}C_{\rm PX} \tag{1}$$

where  $N_{\rm H} \equiv S_{\rm H}/P$  is the number of pixels per scan line. The factor of 9 accounts for the fact that each pixel consists of three subpixels of the primary colors. In this nomenclature,  $R_{\rm PX}$  and  $C_{\rm PX}$  are the respective resistance and capacitance per subpixels.

If the scan line is addressed using drivers from its two ends, then only half of the pixels  $N_{\rm H}/2$  needs to be addressed from each end, the resulting reduced time constant, denoted by  $T^*_{RC}$ , is given by

$$T_{RC}^* \approx \frac{9}{4} N_{\rm H}^2 R_{\rm PX} C_{\rm PX}.$$
 (2)

With  $W_{SC}$  and  $R'_s$  denoting, respectively, the width and the sheet resistance of the scan line, the one obtains

$$R_{\rm PX} = \frac{P}{3W_{\rm SC}} R'_{\rm s} = \frac{S_{\rm H}}{3N_{\rm H}W_{\rm SC}} R'_{\rm s}.$$
 (3)

If the width of the data line is denoted by  $W_{\text{DT}}$ , then  $W_{\text{SC}}W_{\text{DT}}$  are the area of the crossover between the scan line and data line. This contributes a crossover capacitance of  $W_{\text{SC}}W_{\text{DT}}C'_{\text{X}}$  to  $C_{\text{PX}}$ , where  $C'_{\text{X}}$  is the crossover capacitance per unit area. The capacitive loading on the scan line attributed to the address TFT with width W and gate length  $L_g$  is  $WL_gC'_{\text{GI}}$ , where  $C'_{\text{GI}}$  is the gate insulator capacitance per unit area. Consequently,

$$C_{\text{PX}} = \underbrace{W_{\text{SC}}W_{\text{DT}}C'_{\text{X}}}_{\text{Cross-over}} + \underbrace{WL_{g}C'_{\text{GI}}}_{\text{Address-TFT}}.$$
(4)

Substituting (3) and (4) into (2), one obtains

$$T_{RC}^* \approx \frac{3}{4} R_{\rm s}'(N_{\rm H}S_{\rm H}) \left( W_{\rm DT}C_{\rm X}' + \frac{W}{W_{\rm SC}} L_{\rm g}C_{\rm GI}' \right).$$
(5)

For the popular display format of 16:9, the number of scan lines is  $N_V = (9/16)N_H$ . Denoting the frame rate by f, one obtains an upper bound for  $T_{RC}^*$ 

$$T_{RC}^* < \eta \frac{1}{fN_{\rm V}} \tag{6}$$

where  $\eta < 1$  is included to account for the finite time required to pass the signal on the data line to the pixel by the address-TFT.

Adopting  $\eta = 1/4$  [27] and substituting (5) into (6), one obtains after rearranging terms

$$\underbrace{\aleph \equiv R_{\rm s}'\left(W_{\rm DT}C_{\rm X}' + \frac{W}{W_{\rm SC}}L_{\rm g}C_{\rm GI}'\right)}_{\text{Material selection}} < \Box \equiv \underbrace{\frac{16}{27}\left(\frac{1}{fN_{\rm H}^2s_{\rm H}}\right)}_{\text{Display}}_{\text{Specification}}.$$
(7)

The LHS of (7) is denoted by  $\aleph$  and related to the pixel design through various widths, the transistor architecture through  $L_g$  and the technology through the selection of materials. The RHS is denoted by  $\square$  and related to the display specification.



Fig. 2. Schematic cross sections of (a) ES, (b) BCE, and (c) TSA address-TFT.

The *RC* delay attributed to the crossover between the scan line and data line is proportional to  $W_{\text{DT}}$ , and independent of  $W_{\text{SC}}$ ; that attributed to the address-TFT depends on the TFT architecture primarily through  $L_g$ . For a given interconnect geometry, both are reduced by employing a conductor (such as Cu) with lower resistivity. To the extent possible to maximize the aperture ratio of a pixel,  $W_{\text{DT}}$  and  $W_{\text{SC}}$  are set to  $\lambda$  in the present analysis. In practice and if required, each could be suitably enlarged at the expense of smaller aperture ratio to better accommodate, respectively, the data line delay and the charging of the address-TFT. Depending on the value of  $L_g$ , W is adjusted accordingly to achieve the same current drive [28].

Since  $C'_{\text{GI}} \ge C'_{\text{X}}$  in practice, *RC* delay is often dominated by that attributed to the address-TFT. It is for this reason that a TFT architecture allowing a small  $L_{\text{g}}$  is advantageous in reducing the overall signal delay. Shown in Fig. 2 is the cross-sectional schematics of the conventional back-channeletched (BCE) and ES bottom-gate TFT architectures, and the SA, top-gate (TSA) TFT architecture.

It is noted that because of alignment requirement, the respective minimum  $L_g$  is  $3\lambda$ ,  $5\lambda$ , and  $\lambda$  for the BCE, ES, and TSA TFT (Fig. 2). The TSA architecture further allows the placement of the data line above the planarization layer, resulting in a thicker insulation (hence smaller  $C'_X$ ) between the data line and scan line. The parameters used in the present analysis are summarized in Table I.

Shown in Fig. 3 is the dependence of on display diagonal size (~1.15  $S_{\rm H}$  for a 16:9 format) with  $N_{\rm H} = 4$ K (i.e., 3840) or 8K (i.e., 7680), all driven at f = 120 Hz. According to (7),  $\Box$  decreases linearly with the display size but quadratically with  $N_{\rm H}$ . Consequently, there is a more significant decrease in  $\Box$  with an increase of  $N_{\rm H}$  from 4K to 8K.

TABLE I PARAMETERS USED FOR  $T^*_{RC}$  ESTIMATION [29]–[31], ASSUMING  $\lambda = 4 \ \mu m$ 

Parameters	Unit	ES	BCE	TSA
$R'_{\rm s}$	Ω	0.04	0.04	0.04
$C_{ m X}^{'}$	aF/µm <sup>2</sup>	99	173	23
$C_{ m GI}^{'}$	aF/µm <sup>2</sup>	173	173	173
$L_{ m g}$	μm	5λ	3λ	λ
W	μm	$3\lambda$	λ	λ



Fig. 3. Dependence of  $\exists$  on display diagonal size with  $N_{\rm H} = 4$ K or 8K and f = 120 Hz.  $\otimes$  for different TFT architectures are also indicated.



Fig. 4. Schematic cross section of an SA EMMO address-TFT.

The relatively large feature size of the ES architecture precludes its application in an 8K display. The BCE architecture fares better, but only for diagonal size up to about 30 in. Though this size limit could be raised by adopting more advanced driving techniques [32], it is clear that the BCE architecture is not the most versatile condidate for 8K displays. The TSA TFT technology is clearly superior: enabled by the small size of the address-TFT and the small  $C'_X$ , the upper bound for diagonal size is beyond 100 in for f = 120 Hz and  $N_{\rm H} = 8$ K.

While retaining the size advantage of a TSA TFT, there is a desire to overcome its poorer reliability [5] by developing a process to realize an SA, bottom-gate TFT. This is presently implemented based on the EMMO TFT (Fig. 4) architecture.



Fig. 5. Schematic cross section of a windowed bridge structure.

## III. DEPENDENCE OF THE LOCATION OF AN ANNEALING-INDUCED JUNCTION ON THERMAL TREATMENT

A windowed bridge structure (Fig. 5) was used to investigate the relationship between the thermal treatment and the location of an annealing-induced junction. A window was opened in the top layer of gas-impermeable silicon nitride ( $SiN_x$ ), thus allowing oxidation of the IGZO layer covered under the exposed layer of gas-permeable silicon oxide ( $SiO_y$ ).

Fabrication of the structure started with a heavily doped, n-type silicon substrate covered with 100-nm-thick thermal oxide. A stack of insulating films consisting of 75-nm-thick  $SiO_y$  on a 50-nm-thick  $SiN_x$  was deposited by plasmaenhanced chemical vapor deposition (PECVD). The respective carrier gases were 8-SCCM silane/1400-SCCM nitrous oxide and 40-SCCM silane/40-SCCM ammonia; the temperature was 300 °C, and the pressure was 0.9 Torr.

A 20-nm-thick IGZO active layer was subsequently deposited at room temperature in a radio frequency magnetron sputtering machine at a process pressure of 3 mTorr in an atmosphere of 5% oxygen (O<sub>2</sub>) and 95% argon. The molar ratio of the IGZO target was  $In_2O_3$ :Ga<sub>2</sub>O<sub>3</sub>:ZnO = 1:1:1, and the base pressure was ~1 µTorr. An active island of width  $W_{IS}$  was patterned using 1/1000 molar aqueous hydrofluoric acid solution, before a 300-nm-thick gas-permeable SiO<sub>y</sub> passivation layer and an 80-nm-thick gas-impermeable SiN<sub>x</sub> cover layer were sequentially deposited using the same PECVD processes.

The SiN<sub>x</sub> cover layer was patterned and a window of length  $L_A$  and width >  $W_{IS}$  was opened by etching in an inductively coupled plasma etcher running a sulfur hexafluoride chemistry, thus exposing the underlying SiO<sub>y</sub> passivation layer in the windows. Contact holes were subsequently opened before the metal electrodes, consisting of sputtered and patterned stacks of 300-nm-thick aluminum (Al) on a 50-nm-thick Mo, were defined. Finally, the devices were annealed in a conventional resistively heated horizontal atmospheric pressure furnace at 400 °C for 2 h with an N<sub>2</sub> flow rate of 8 SLPM.

Electrical characteristics were measured using an Agilent 4156C semiconductor parameter analyzer. Recognizing the similarity between the bridge structure and a bottom-gate TFT, one can modulate the conductance of the IGZO in the window by applying a "gate" bias  $V_g$  to the heavily doped silicon substrate. In this analogy, the conductive regions on the two



Fig. 6.  $R_{\rm T}$  of the bridge structure after various thermal treatment of (a) 2 h N<sub>2</sub>-annealing, (b) 2 h O<sub>2</sub>-annealing, (c) 5 h O<sub>2</sub>-annealing, and (d) 8 h O<sub>2</sub>-annealing as a function of drawn  $L_{\rm A}$  for a different  $V_{\rm g}$ . Each corresponding  $\Delta L_{\rm A}$  is extracted from the intersection of the lines.

sides of the IGZO active layer in the window are equivalent to the S/D regions of the TFT.

Consistent with the formation mechanism of annealinginduced donor defects under the condition of nonoxidizing heat treatment, the edge (thus junction) of a conductive region is largely aligned to the corresponding edge of the gasimpermeable SiN<sub>x</sub> cover layer. With the misalignment between these edges denoted by  $\Delta L_A$ , the total resistance  $R_T$  measured between the metal-to-S/D contacts is given by [33], [34]

$$R_{\rm T} = \frac{L_{\rm A} - 2\Delta L_{\rm A}}{W_{\rm IS}} \left( R'_{\rm A} - R'_{\rm S/D} \right) + \frac{L_{\rm C}}{W_{\rm IS}} R'_{\rm S/D}$$
(8)

where  $L_{\rm C} = 300 \ \mu {\rm m}$  is the separation between the contacts;  $R'_{\rm A}$  and  $R'_{\rm S/D}$  are the respective sheet resistance of the IGZO active layer in the window and in the adjoining equivalent S/D regions. The dependence of  $R_{\rm T}$  on  $L_{\rm A}$  and  $V_{\rm g}$  after the initial 2 h, N<sub>2</sub>-annealing at 400 °C is displayed in Fig. 6(a). The relatively constant  $R_{\rm T}$  implies  $R'_{\rm A} \approx R'_{\rm S/D}$ . This is reasonable since the IGZO inside the window was also subjected to a nonoxidizing anneal, resulting in the creation of donor defects, the large population of which is relatively insensitive to further modulation by  $V_{\rm g}$ .

This population decreases after a subsequent oxidizing anneal in the same furnace and when it becomes negligible compared to the field-effect-induced population, one obtains

$$R'_{\rm A} \approx \frac{1}{\mu_{\rm FE} C'_{\rm GI} (V_{\rm g} - V_{\rm T})}.$$
(9)

It should be noted that  $(V_g - V_T) \gg V_d$  is assumed in (9), where  $V_d$  is the bias applied to the D electrode (Fig. 5).



Fig. 7. Dependence of  $\Delta L_A$  on a different O<sub>2</sub>-annealing time.

Consequently

$$R_{\rm T} \approx \frac{L_{\rm A} - 2\Delta L_{\rm A}}{W_{\rm IS}} \left[ \frac{1}{\mu_{\rm FE} C'_{\rm GI} (V_{\rm g} - V_{\rm T})} - R'_{\rm S/D} \right] + \frac{L_{\rm C}}{W_{\rm IS}} R'_{\rm S/D}.$$
(10)

Typical dependence of  $R_{\rm T}$  on  $L_{\rm A}$  and  $V_{\rm g}$  after a series of oxidizing thermal treatments with increasing duration is displayed in Fig. 6.  $V_{\rm g}$  was varied between 18 and 22 V, and  $V_{\rm d}$  was fixed at 0.5 V.

For the initial state after the N<sub>2</sub>-annealing, the entire IGZO active layer was populated by donor defects [inset of Fig. 6(a)] without any junctions separating the "channel" in the window and the adjacent equivalent "S/D" regions. For each duration of O<sub>2</sub>-annealing at 400 °C, a unique  $\Delta L_A$  can be extracted from the common intersection of the least-square fitting lines at various values of  $V_g$ . The dependence of  $\Delta L_A$  on the O<sub>2</sub>-annealing time (Fig. 7) can be roughly divided into two regimes, with  $\Delta L_A$ , respectively, changing more quickly for annealing time less than 4 h and slower for longer annealing time.

During the subsequent short-duration oxidizing anneal, O<sub>2</sub> entered the thin 20-nm IGZO in the window and annihilated the donor defects. Since the entire surface of the channel is "exposed" to O<sub>2</sub> diffusing through the SiO<sub>y</sub> passivation layer, this is a regime characterized by "vertical" oxidation. The annihilation in the edge regions is incomplete during this short-duration anneal due to the supply of donor defects from the SiN<sub>x</sub>-covered equivalent S/D regions, resulting in a small but positive  $\Delta L_A$  (inset I). Upon further annealing beyond 3.5 h, the defect-annihilation fronts (hence junctions) were pushed into the SiN<sub>x</sub>-covered regions.  $\Delta L_A$  turned negative (Inset II) and its time rate of change slowed down appreciably. This is a regime characterized by "lateral" oxidation, hence annihilation, of the donor defects.

## IV. SELF-ALIGNED EMMO TFTS USING BACK-SIDE EXPOSSURE

The deeper knowledge gained on how a thermal treatment affects the alignment between an induced junction and the corresponding edge of a  $SiN_x$  gas-impermeable cover was applied



Fig. 8. Schematic process flow for the realization of an SA EMMO IGZO TFT using back-side exposure. (a) Back-side flood-exposure. (b) Window area patterning. (c) Contact region opening. (d) Metal electrode definition and S/D formation.

to the construction of an SA, bottom-gate TFT based on the EMMO architecture [35]. The fabrication of the TFT started with the sputter deposition and patterning of 120-nm-thick Mo gate electrode on a transparent glass substrate. Identical to the process sequence used to construct the bridge structure, the same stack of  $SiO_y/SiN_x$  gate insulator, IGZO semiconductor, gas-permeable  $SiO_y$  passivation layer, and gas-impermeable  $SiN_x$  cover layer were deposited and patterned.

A negative-tone photoresist layer was subsequently coated on the cover layer before it was flood exposed from the back side [Fig. 8(a)], thus capturing the image of the opaque gate electrode. A window was etched through the exposed cover layer [Fig. 8(b)] to reveal the underlying SiO<sub>y</sub> passivation layer. The edges of the window along the channel direction were self-aligned to those of the gate electrode. Contact regions exposing the IGZO active layer on the two sides were opened [Fig. 8(c)], before the S/D electrodes consisting of the same stack of Al on Mo were patterned. Finally, conductive S/D regions self-aligned to the edges of the cover layer, hence also to those of the gate electrode, were formed after a thermal treatment at 400 °C in O<sub>2</sub> [Fig. 8(d)].

With an overlap of  $\sim 4 \ \mu m$  between the gate and the S/D electrode, regular EMMO TFTs with lithographically defined S/D electrodes were also constructed for comparison.  $V_{\rm g}$ -dependent gate capacitance of the regular and SA TFTs is compared in Fig. 9 for TFTs with different channel length L.

The values at sufficiently negative  $V_g$  are insensitive to L and provide estimates of the parasitic gate-junction capacitance of ~241 and ~30 fF, respectively, for the regular and the SA TFTs. Clearly the parasitic capacitance of the latter, at merely ~13% of that of the former, is much smaller.

Shown in the Fig. 10 is drain current  $(I_d)$  versus  $V_g$  transfer characteristics of SA EMMO TFTs with a different W at the same  $L = 5 \ \mu\text{m}$ . From the peak transconductance  $(g_m)$ measured at a  $V_d$  of 0.5 V, a  $\mu_{FE} \ \equiv Lg_m/WC'_{GI}V_d$ ) of 5.8  $\pm$  0.4 cm<sup>2</sup>/Vs was extracted. A maximum subthreshold slope of 372  $\pm$  27 mV/decade was extracted at  $V_g$  larger than the turn-ON voltage  $V_{ON} \ \equiv V_g$  to induce an  $I_d$  of  $L/W \times 10$  nA at  $V_d = 5$  V). All devices exhibit relatively low OFF-state current of  $\sim 10^{-13}$  A, hence a high ON-/OFF-current ratio of at least 10<sup>9</sup>. This is consistent with the effectiveness of thermal oxidation in reducing the defect concentration in an



Fig. 9. Capacitance–voltage characteristics of regular (Reg) and SA EMMO TFTs with two different values of *L*.



Fig. 10. Transfer characteristics of SA EMMO IGZO TFTs at  $V_d = 5$  V with different channel widths. Inset: dependence of normalized  $I_{ON}$  on a different annealing time.

MO semiconductor. The performance of the SA EMMO TFTs is comparable to that previously reported for bottom-gate SA MO TFTs [18], [22].

Shown in the inset of Fig. 10 is the degradation of the normalized "ON" current  $(I_{ON})$  of TFTs subjected to different annealing durations. Compared with  $I_{ON}$  after 1 h of O<sub>2</sub>-annealing at 400 °C, that after 2 h of annealing was slightly reduced. This is related to the continuous migration of the junctions toward to the edges defined by the S/D SiN<sub>x</sub> cover layer, hence a slight increase in the effective *L*. Upon further extending the annealing duration to 4 h and then 6 h, a precipitous drop in  $I_{ON}$  was observed. This is caused by the migration of the junctions to beyond the edges of the gate electrode, thus breaking the connection between the field-induced channel and the annealing-induced S/D regions. In the present demonstration, annealing at 400 °C in O<sub>2</sub> between 1 and 3 h appears acceptable, reflecting a fairly wide process window.

## V. CONCLUSION

It is shown that the gate-junction overlap capacitance of a TFT makes a significant contribution to the capacitive loading of a scan line in a matrix display employing the traditional bottom gate, staggered transistor architectures. The increased signal delay along the line, if not mitigated, also constrains the construction of large-area, high-resolution, and highframe-rate displays. The process dependence of the migration of an annealing-induced junction in IGZO is studied and characterized. The insight acquired is applied to the construction of a bottom-gate transistor with annealing-induced junctions self-aligned to the edges of the gate electrode, employing merely an additional maskless, back-side flood exposure step. While offering the same small parasitic capacitance as that of an SA, top-gate transistor, this SA, bottom-gate technology further allows full oxidation of the channel region-thus improving the performance and reliability of the transistor.

## ACKNOWLEDGMENT

The authors would like to thank the assistance of the Nanosystem Fabrication Facility, The Hong Kong University of Science and Technology, Hong Kong, in device fabrication.

#### REFERENCES

- R. Hayashi *et al.*, "Improved amorphous In-Ga-Zn-O TFTs," in SID Symp. Dig. Tech. Papers, May 2008, vol. 39. no. 1, pp. 621–624, doi: 10.1889/1.3069739.
- [2] M. Kim *et al.*, "High mobility bottom gate InGaZnO thin film transistors with SiO<sub>x</sub> etch stopper," *Appl. Phys. Lett.*, vol. 90, no. 21, p. 212114, May 2007, doi: 10.1063/1.2742790.
- [3] T. Arai and T. Sasaoka, "Emergent oxide TFT technologies for nextgeneration AM-OLED displays," in *SID Symp. Dig. Tech. Papers*, Jun. 2011, vol. 42. no. 1, pp. 710–713, doi: 10.1889/1.3621424.
- [4] R. Chaji and A. Nathan, "LTPS vs oxide backplanes for AMOLED displays: System design considerations and compensation techniques," in *SID Symp. Dig. Tech. Papers*, Jun. 2014, vol. 45. no. 1, pp. 153–156, doi: 10.1002/j.2168-0159.2014.tb00042.x.
- [5] H.-J. Shin *et al.*, "Novel OLED display technologies for large-size UHD OLED TVs," in *SID Symp. Dig. Tech. Papers*, Jun. 2015, vol. 46. no. 1, pp. 53–56, doi: 10.1002/sdtp.10225.
- [6] E. Fortunato, P. Barquinha, and R. Martins, "Oxide semiconductor thin-film transistors: A review of recent advances," *Adv. Mater.*, vol. 24, no. 22, pp. 2945–2986, Jun. 2012, doi: 10.1002/adma.201103228.
- [7] J. S. Park, W.-J. Maeng, H.-S. Kim, and J.-S. Park, "Review of recent developments in amorphous oxide semiconductor thin-film transistor devices," *Thin Solid Films*, vol. 520, no. 6, pp. 1679–1693, Jan. 2012, doi: 10.1016/j.tsf.2011.07.018.
- [8] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 4016, pp. 488–492, Nov. 2004, doi: Doi.10.1038/Nature03090.
- [9] C.-W. Han *et al.*, "Advanced technologies for large-sized OLED TV," in *SID Symp. Dig. Tech. Papers*, Jun. 2014, vol. 45. no. 1, pp. 770–773, doi: 10.1002/j.2168-0159.2014.tb00202.x.
- [10] C.-H. Oh, H.-J. Shin, W.-J. Nam, B.-C. Ahn, S.-Y. Cha, and S.-D. Yeo, "Technological progress and commercialization of OLED TV," in *SID Symp. Dig. Tech. Papers*, Jun. 2013, vol. 44. no. 1, pp. 239–242, doi: 10.1002/j.2168-0159.2013.tb06189.x.
- [11] M. D. H. Chowdhury, P. Migliorato, and J. Jang, "Low temperature characteristics in amorphous indium-gallium-zinc-oxide thin-film transistors down to 10 K," *Appl. Phys. Lett.*, vol. 103, no. 15, pp. 1–5, 2013, doi: 10.1063/1.4824875.
- [12] J. K. Jeong *et al.*, "12.1-inch WXGA AMOLED display driven by indium-gallium-zinc oxide TFTs array," in *SID Symp. Dig. Tech. Papers*, May 2008, vol. 39. no. 1, p. 1–4, doi: 10.1889/1.3069591.

- [13] N. Morosawa, Y. Ohshima, M. Morooka, T. Arai, and T. Sasaoka, "A novel self-aligned top-gate oxide TFT for AM-OLED displays," in *SID Symp. Dig. Tech. Papers*, Jun. 2011, vol. 42. no. 1, pp. 479–482, doi: 10.1889/1.3621360.
- [14] S. Kim *et al.*, "Source/drain formation of self-aligned top-gate amorphous GaInZnO thin-film transistors by NH<sub>3</sub> plasma treatment," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 374–376, Apr. 2009, doi: 10.1109/LED.2009.2014181.
- [15] K. H. Ji, J. Noh, P. S. Yun, J. U. Bae, K.-S. Park, and I. Kang, "P-2: Novel high mobility oxide TFT with self-aligned s/d regions formed by wet-etch process," *SID Symp. Dig. Tech. Papers*, vol. 47, no. 1, pp. 1129–1131, May 2016, doi: 10.1002/sdtp.10820.
- [16] R. Chen, W. Zhou, M. Zhang, M. Wong, and H. S. Kwok, "Self-aligned indium-gallium-zinc oxide thin-film transistor with source/drain regions doped by implanted arsenic," *IEEE Electron Device Lett.*, vol. 34, no. 1, pp. 60–62, Jan. 2013, doi: 10.1109/LED.2012.2223192.
- [17] S.-M. Ryu, M.-H. Kim, S.-H. Jeon, J.-H. Lim, and D.-K. Choi, "selfaligned coplanar top gate In-Ga-ZnO thin-film transistors exposed to various DUV irradiation energies," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 1–5, Aug. 2016, doi: 10.1109/TED.2016.2575001.
- [18] M. Nakata, H. Tsuji, Y. Fujisaki, Y. Nakajima, T. Takei, and T. Yamamoto, "Electrical and structural characterization of self-aligned InGaZnO thin-film transistors fabricated by excimer laser irradiation," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5972–5977, Nov. 2017, doi: 10.1109/TIA.2017.2726504.
- [19] D. H. Kang, I. Kang, S. H. Ryu, and J. Jang, "Self-aligned coplanar a-IGZO TFTs and application to high-speed circuits," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1385–1387, Oct. 2011, doi: 10.1109/LED.2011.2161568.
- [20] L. Lu and M. Wong, "A bottom-gate indium-gallium-zinc oxide thinfilm transistor with an inherent etch-stop and annealing-induced source and drain regions," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 574–579, Feb. 2015, doi: 10.1109/TED.2014.2375194.
- [21] L. Lu, J. Li, and M. Wong, "A comparative study on the effects of annealing on the characteristics of zinc oxide thin-film transistors with gate-stacks of different gas-permeability," *IEEE Electron Device Lett.*, vol. 35, no. 8, pp. 841–843, Aug. 2014, doi: 10.1109/LED.2014. 2326960.
- [22] J. Jiang, M. Furuta, and D. Wang, "Self-aligned bottom-gate In-Ga-Zn-O thin-film transistor with source/drain regions formed by direct deposition of fluorinated silicon nitride," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 933–935, Sep. 2014, doi: 10.1109/LED.2014.2336880.
- [23] L. Lu and M. Wong, "The resistivity of zinc oxide under different annealing configurations and its impact on the leakage characteristics of zinc oxide thin-film transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1077–1084, Apr. 2014, doi: 10.1109/TED.2014.2302431.
- [24] Z. Xia *et al.*, "Characteristics of elevated-metal metal-oxide thin-film transistors based on indium-tin-zinc oxide," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 894–897, Jul. 2017, doi: 10.1109/LED.2017.2707090.
- [25] L. Lu, J. Li, H. S. Kwok, and M. Wong, "High-performance and reliable elevated-metal metal-oxide thin-film transistor for highresolution displays," in *IEDM Tech. Dig.*, Dec. 2017, pp. 32.2.1–32.2.4, doi: 10.1109/IEDM.2016.7838526.
- [26] T. Sakurai, "Approximation of wiring delay in MOSFET LSI," *IEEE J. Solid-State Circuits*, vol. 18, no. 4, pp. 418–426, Aug. 1983, doi: 10.1109/JSSC.1983.1051966.
- [27] A. Kumar *et al.*, "Design considerations for active matrix organic light emitting diode arrays," *IEE Proc.-Circuits, Devices Syst.*, vol. 150, no. 4, pp. 322–328, Aug. 2003, doi: 10.1049/ip-cds:20030730.
- [28] J. Li, L. Lu, Z. Xia, H. S. Kwok, and M. Wong, "Three-mask elevatedmetal metal-oxide thin-film transistor with self-aligned definition of the active island," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 35–38, Jan. 2018, doi: 10.1109/LED.2017.2775041.
- [29] S.-M. Ge et al., "Development of Cu BCE-structure IGZO TFT for a high-ppi 31-in. 8K × 4K GOA LCD," in SID Symp. Dig. Tech. Papers, May 2017, vol. 48. no. 1, pp. 592–595, doi: 10.1002/sdtp.11705.
- [30] Y. G. Mo *et al.*, "Amorphous oxide TFT backplane for large size AMOLED TVs," in *SID Symp. Dig. Tech. Papers*, May 2010, vol. 41, no. 1, p. 1037, doi: 10.1889/1.3499826.
- [31] W. den Boer, *Active Matrix Liquid Crystal Displays* (Fundamentals and Applications). Richmond, U.K.: Newens, 2005.
- [32] T. Kumakura, S. Yoshida, A. Tomiyoshi, T. Fujine, and Y. Yoshida, "Development of a novel wide- gamut 8 K 120 Hz LCD complying with ITU-r BT.2020," in *SID Symp. Dig. Tech. Paperas*, Jun. 2015, vol. 46. no. 1, pp. 1070–1073, doi: 10.1002/sdtp.10396.

- [33] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho, "A new method to determine MOSFET channel length," *IEEE Electron Device Lett.*, vol. EDL-1, no. 9, pp. 170–173, Sep. 1980, doi: 10.1109/EDL.1980.25276.
- [34] Y. Taur, "MOSFET channel length: Extraction and interpretation," *IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 160–170, Jan. 2000, doi: 10.1109/16.817582.
- [35] L. Lu, J. Li, Z. Feng, H.-S. Kwok, and M. Wong, "Elevated-metal metaloxide (EMMO) thin-film transistor: Technology and characteristics," *IEEE Electron Device Lett.*, vol. 37, no. 6, pp. 728–730, Jun. 2016, doi: 10.1109/LED.2016.2552638.



Zhihe Xia received the B.S. degree in optical information science and technology from the Huazhong University of Science and Technology, Wuhan, China, in 2013. He is currently pursuing the Ph.D. degree with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong.

His current research interests include indiumgallium-zinc oxide thin-film transistors (TFTs) and indium-tin-zinc oxide TFTs with advanced device architectures.



Lei Lu (M'17) received the Ph.D. degree from the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, in 2016.

His current research interests include novel thin-film transistor (TFT) structures and oxide TFTs.



Jiapeng Li is currently pursuing the Ph.D. degree with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong.

His current research interests include oxide thin-film transistor and its reliability.



**Hoi-Sing Kwok** (M'78–SM'84–F'05) received the Ph.D. degree in applied physics from Harvard University, Cambridge, MA, USA, in 1978.

He joined The Hong Kong University of Science and Technology, Hong Kong, in 1992, where he is currently the Director of the Center for Display Research and the State Key Laboratory on Advanced Displays and Optoelectronics Technologies.



Man Wong (M'84–SM'00) received the Ph.D. degree in electrical engineering from the Center for Integrated Systems, Stanford University, Palo Alto. CA. USA.

In 1992, he joined the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Hong Kong, as a Faculty Member.