Suppressed Degradation of Elevated-Metal Metal–Oxide Thin-Film Transistors Under Bipolar Gate Pulse Stress

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***Abstract*— In this letter, investigations on the reliability of elevated-metal metal–oxide (EMMO) thin-film transistors (TFTs) under bipolar gate pulse stress are reported. Different from conventional amorphous indium–gallium–zinc oxide TFTs, EMMO TFTs exhibit negligible dynamic degradation during the pulse transitions and the device degradation is dominated by the DC mechanism. Though negative threshold voltage (V_{th}) shift is observed under both positive bias stress (PBS) and negative bias stress, the V_{th} shift caused by the bipolar pulse stress is smaller than that induced by the PBS with the same positive gate bias as in the bipolar gate pulse and the same effective PBS time, where the V_{th} shift introduced during the positive bias stage in the bipolar pulse stress is believed to be partially recovered during the negative bias stage. These degradation phenomena are proposed to be due to the improved quality of the channel and the gate oxide with the oxidizing thermal heat-treatment during the fabrication of EMMO TFTs, which eventually lead to a reliable performance for the EMMO TFTs under bipolar gate pulse stress.**

***Index Terms*— Elevated-metal metal-oxide, thin-film transistor, gate pulse stress, positive bias stress, negative bias stress.**

I. Introduction

RECENTLY, an elevated-metal metal-oxide (EMMO) thin-film transistor (TFT) structure with an oxidizing heat-treatment process is proposed. The EMMO TFT is superior to the conventional back-channel-etched (BCE) or etch-stop (ES) metal-oxide TFT. The EMMO TFT accommodates an ES layer without introducing extra masks by tactfully elevating the source/drain electrodes onto the passivation layer, while the incorporation of annealing-induced source/drain regions retains a small device footprint, making it applicable in high-resolution active-matrix displays [1]. Furthermore, the reduction of defect density in the channel region during the heat-treatment in oxygen atmosphere makes the EMMO TFT of high performance and reliability [2].

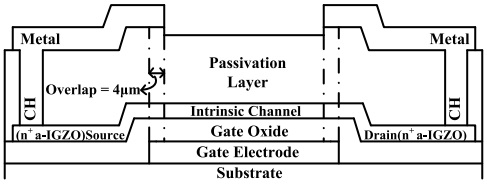

Fig. 1. The schematic cross-section of an EMMO TFT.

In previous work, a considerable amount of efforts have been put on analyzing the device degradation of amorphous indium-gallium-zinc oxide (a-IGZO) TFTs under DC stress, for example, positive bias stress (PBS), negative bias stress (NBS), or their combinations with temperature or illumination [3]–[6]. At the same time, because TFTs are frequently subjected to pulse voltages and switch between on and off states in active-matrix display applications, more and more researchers are engaged in dynamic stress degradation study [7]–[10]. Recently, the high reliability of EMMO TFTs under DC bias stress has been reported [1], while the degradation under dynamic bias stress which possesses great practical significance is not involved yet. In this work, the degradation behaviors of EMMO TFTs under bipolar gate pulse stress are reported. Negligible degradation occurred at transient time of the pulse stress for EMMO TFTs is observed and reported for the first time, whereas the dynamic degradation is the dominant one for conventional TFTs. Though the degradation of EMMO TFTs under bipolar gate pulse stress is dominated by the DC bias stress and V_{th} both shifts negatively after PBS and NBS, the negative shift of V_{th} after bipolar gate pulse stress is still smaller than that after PBS with the same positive gate bias as in the pulse stress and the same effective PBS time. From the mechanism point of view, compensation effect between PBS and NBS periods in the bipolar pulse stress for the EMMO TFTs is proposed.

II. Experiments

Device structure for the inverted-staggered bottom gate EMMO TFTs used in this work is schematically shown in Fig. 1. The indium-tin oxide was first sputtered and patterned as the gate electrode, and then a 100 nm silicon dioxide (SiO_2) gate insulator was deposited by low pressure chemical vapor deposition (LPCVD), followed by a 30 nm a-IGZO

Manuscript received March 20, 2018; accepted March 27, 2018. Date of publication March 30, 2018; date of current version April 24, 2018. This work was supported in part by the Science and Technology Program of Suzhou city under Grant SYG201538 and in part by the National Natural Science Foundation of China under Grant 61574096. The review of this letter was arranged by Editor A. Chin. *(Corresponding author: Dongli Zhang.)*

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Digital Object Identifier 10.1109/LED.2018.2821366

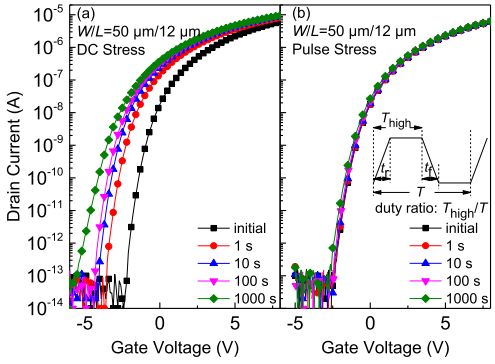

Fig. 2. The time evolution of transfer characteristics of EMMO TFTs under (a) DC stress with $V_g = 40$ V, (b) gate pulse stress, V_g pulses swinging between -22 V and 18 V, which is symmetric about the V_{FB} of -2 V.

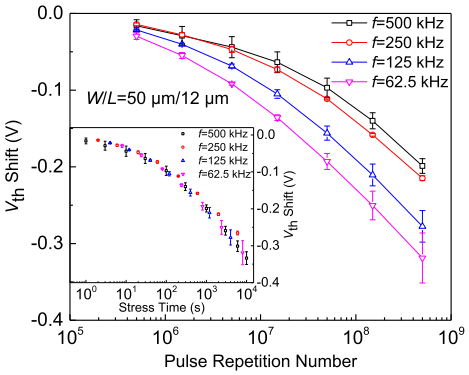

Fig. 3. Dependence of V_{th} shift on pulse repetition number under different frequencies. The inset shows the dependence of V_{th} shift on stress time.

active layer deposition by radio-frequency (RF) magnetron sputtering at room temperature. Subsequently, a 300 nm SiO_2 passivation layer was deposited by LPCVD. Then the contact holes were opened and a molybdenum/aluminum (Mo/Al) bilayer was patterned to form the source/drain electrodes, which have 4 μm overlap with the gate electrode. Crucially, a heat-treatment in O_2 was then carried out at 400 °C for 2 hours to form the conductive source/drain regions, which also improves the quality of the channel a-IGZO and the gate insulator [2].

The transfer characteristics of the EMMO TFTs before and after stress are measured with Agilent 4156C semiconductor parameter analyzer. All the reliability experiments are carried out at room temperature, and for the gate bias stress experiments, the source/drain electrodes are grounded. For the bipolar gate voltage (V_g) pulse stress, symmetrical pulse stress about the flat-band voltage (V_{FB}) is chosen [11], and the V_{FB} is defined as the V_g at the transition point between subthreshold region and off-state region in the transfer characteristics. The rising time (t_r) and falling time (t_f) are both 100 ns, the duty ratio is 50%. All the transfer characteristics are measured at $V_{ds} = 5$ V, and the device degradation is characterized by V_{th} shift from its initial value, where V_{th} is defined as the V_g when the drain current normalized by the ratio W/L reaches 10 nA in the transfer curve.

III. Results and Discussion

We first compared the device degradation of EMMO TFTs under DC and pulse V_g stress with the same amplitude [11]. Fig. 2(a) shows the evolution of transfer characteristics for EMMO TFTs after PBS with a relatively high V_g stress of +40 V. With the increase of stress time, an obvious negative shift of transfer characteristics is observed. For the pulse V_g stress, the V_g pulses swing between -22 V and 18 V with the same amplitude of 40 V, the frequency $f = 500$ kHz. As shown in Fig. 2(b), one can notice that a minimal negative shift of transfer characteristics occurs. After the same stress duration of 1000 s, the V_{th} shifts under DC and pulse V_g stress are -2.23 V and -0.20 V, respectively. Obviously, EMMO TFTs degrade much less under pulse bias stress than DC bias stress, which is contrary to the degradation phenomena observed on conventional a-IGZO TFTs [11].

To reveal the mechanism for the suppressed degradation of EMMO TFTs under bipolar gate pulse stress, we first investigated the relationship between the degradation and the pulse transition, where frequency of gate pulses varies from 62.5 kHz to 500 kHz while all other pulse parameters are fixed, i.e., the gate bias swings between -22 V$\sim$18 V with a duty ratio of 50%, and t_r, t_f are 100 ns. Therefore, within the same stress period, the pulse repetition number varies with frequency while the equivalent DC stress duration is the same. As shown in Fig. 3, with the decrease of the pulse frequency, much enhanced degradation occurs at the same pulse repetition number due to the increased equivalent DC stress time. However, if V_{th} shift is replotted versus stress time as the figure inset shows, all degradation curves are overlapped. The observation clearly suggests that the degradation of EMMO TFTs under bipolar gate pulse stress is dominated by the DC mechanism, and the pulse transitions play a negligible role, which distinctly differs from the previous reports on the degradation of conventional a-IGZO TFTs under bipolar gate pulse stress [9], [11].

According to previous reports [11], [12], the degradation mechanism involved during gate pulse stress is that electrons emitted from deep trap states would be exposed to the transient lateral coupled electric field and gain enough energy to overcome the interface barrier and inject into the gate insulator during t_f transients. However, on account of the oxidizing heat-treatment process during the fabrication of EMMO TFTs, the defects in the channel are effectively suppressed [2], [13], which effectively impedes the occurrence of the dynamic hot carrier (HC) effect and thus suppresses the dynamic degradation. For further proof, the worst DC HC stress is carried out on the EMMO TFTs where the V_g is of about V_{th} while with a high V_d [14]. As expected, DC HC stress induced degradation is also suppressed as shown in Fig. 4(a). For the case of DC bias stress with both high V_g and V_d, i.e., $V_g = V_d = 30$ V, as Fig. 4(b) shows, the transfer characteristics shift negatively, and the negative shift of V_{th} is only -0.66 V after the stress duration of 20000 s, which is obviously less than the degradation reported previously [15]. Considering the high V_g and V_d applied to the EMMO TFT, the degradation is most probably induced by the self-heating effect.

Positive shift of V_{th} is consistently observed for TFTs after PBS [3], [4], [7], which caused by electrons trapped at the interface between the gate insulator and channel and/or injected into the gate insulator. However, a negative V_{th} shift is observed for EMMO TFTs as Fig. 2(a) shows. It is proposed

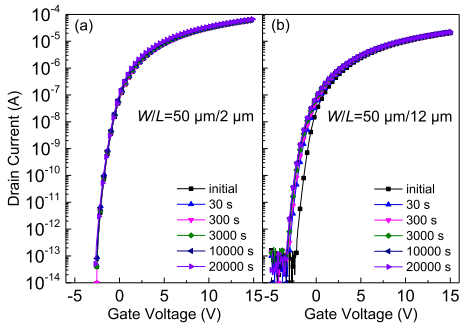

Fig. 4. The time evolution of transfer characteristics of EMMO TFTs under (a) DC HC stress condition ($V_g - V_{th} = 2$ V, $V_d = 30$ V), (b) high gate and drain voltage stress ($V_g = V_d = 30$ V).

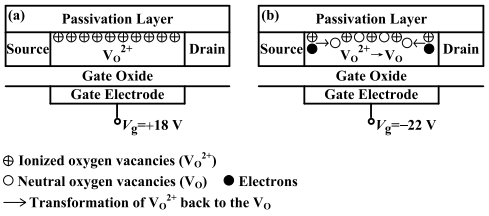

Fig. 5. Degradation model of EMMO TFTs under bipolar gate pulse stress (a) during positive bias stress stage, (b) during negative bias stress stage.

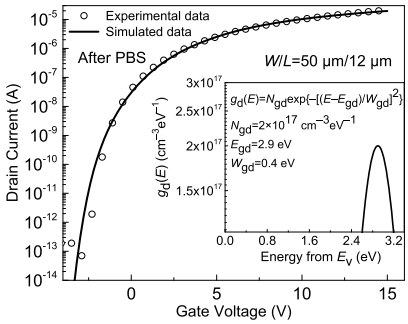

Fig. 6. Comparison of the simulated and measured transfer characteristics of EMMO TFT after 10000 s PBS of 18V. The inset shows the energy band distribution of the added donor-type defects near the conduction band edge.

that due to the improved quality of channel a-IGZO and gate insulator, electron trapping and positive shift of the transfer curves are suppressed. At the same time, the concentration of ionized oxygen vacancies (V_O^{2+}) at the back-channel interface is increased with electrons accumulated to the front channel surface by the vertical electric field [6], as schematically shown in Fig. 5(a), the transfer characteristics thus shift negatively [16]. The proposed mechanism is verified with 2D numerical simulation software Silvaco [17]. As shown in Fig. 6, the transfer characteristics after PBS of 18 V can be well fitted by the addition of donor-like trap states near the conduction band edge within the 10 nm region at the back channel accounting for the V_O^{2+} [18], which follow a Gaussian distribution as $g_d(E) = N_{gd} \exp\{-[(E - E_{gd})/W_{gd}]^2\}$, where N_{gd}, E_{gd} and W_{gd} are 2×10^{17} cm^{-3}eV^{-1}, 2.9 eV and 0.4 eV, respectively. For NBS, negative shift of transfer curves is commonly attributed to the hole trapping in the gate insulator or at the a-IGZO interface [7]. However, due to the high density of donor-like trap states in the bandgap of a-IGZO TFTs [6], the availability of large amount of holes in the a-IGZO is not expected, which is consistent with the negligible

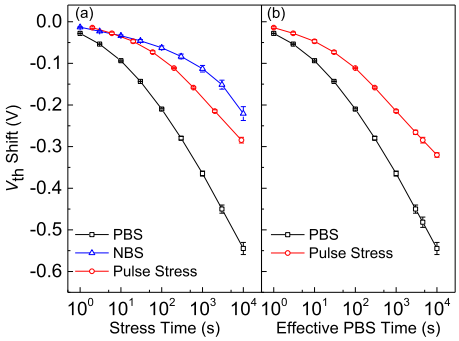

Fig. 7. The V_{th} shift of EMMO TFTs under (a) PBS (+18 V), NBS (−22 V) and bipolar gate pulse stress (−22 V∼ +18 V), respectively, (b) V_{th} shift under PBS (+18 V) and bipolar gate pulse stress (−22 V∼ +18 V) versus the effective PBS time.

negative V_{th} shift under NBS as Fig. 7(a) shows. The gate bias during the NBS is −22 V, which is the same bias voltage as the one in the negative bias stage of the bipolar gate pulse.

Though the degradation induced by the pulse transitions during the bipolar pulse stress is negligible, one can notice in Fig. 7(a) that the V_{th} shift after bipolar gate pulse stress is much smaller than the sum of V_{th} shifts resulted from PBS and NBS during half of the corresponding pulse stress time. For example, after the same stress duration of 3000 s, the respective V_{th} shift for EMMO TFTs under PBS (+18 V) and NBS (−22 V) are −0.45 V and −0.15 V with an overall value of −0.6 V, which is much larger than the V_{th} degradation of −0.27 V under pulse bias stress (−22 V∼ +18 V) after 6000 s. The observed phenomena are attributed to the reduction of the concentration of V_O^{2+} at the back channel, which are formed during the PBS stage in the pulse stress, as electrons move to the back channel and transform part of the V_O^{2+} back to the neutral state (V_O) during the NBS stage in the pulse stress as schematically shown in Fig. 5(b). It is interesting to observe in Fig. 7(b) that the negative shift of V_{th} induced by the PBS is apparently larger than that induced by the bipolar gate pulse stress under the same effective PBS time, which is consistent with the proposed mechanism.

IV. Conclusion

In this letter, some new degradation phenomena under bipolar gate pulse stress are reported for EMMO a-IGZO TFTs. Under the pulse stress, the contribution from dynamic degradation is negligible, which is the dominant one for conventional TFTs, and the negative shift of V_{th} after the pulse stress is smaller than that caused by the PBS with the same effective PBS time. The former is attributed to the improved quality of the channel a-IGZO and the reduced traps state density, and the latter is due to the negative shift of V_{th} induced during the PBS stage in the pulse stress being partially recovered during the NBS stage in the pulse stress. The unique oxidizing heat-treatment process during device fabrication improves the quality of the channel a-IGZO and gate oxide, which in turn ensures the superior stability against bipolar gate pulse stress.

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