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Transistors and tunnel diodes enabled by large-scale MoS_2 nanosheets grown on GaN

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Abstract

We report growth, fabrication, and device results of MoS_2-based transistors and diodes implemented on a single 2D/3D material platform. The 2D/3D platform consists of a large-area MoS_2 thin film grown on SiO_2/p-GaN substrates. Atomic force microscopy, scanning electron microscopy, and Raman spectroscopy were used to characterize the thickness and quality of the as-grown MoS_2 film, showing that the large-area MoS_2 nanosheet has a smooth surface morphology constituted by small grains. Starting from the same material, both top-gated MoS_2 field effect transistors and MoS_2/SiO_2/p-GaN heterojunction diodes were fabricated. The transistors exhibited a high on/off ratio of 10^5, a subthreshold swing of 74 mV dec^{-1}, field effect mobility of 0.17 $cm^2\,V^{-1}\,s^{-1}$, and distinctive current saturation characteristics. For the heterojunction diodes, current-rectifying characteristics were demonstrated with on-state current density of 29 A cm^{-2} and a current blocking property up to −25 V without breakdown. The reported transistors and diodes enabled by the same 2D/3D material stack present promising building blocks for constructing future nanoscale electronics.

Supplementary material for this article is available online

Keywords: 2D material, chemical vapor deposition (CVD), field effect transistors (FETs), heterojunction diode, MoS_2

(Some figures may appear in colour only in the online journal)

1. Introduction

Two-dimensional (2D) semiconducting transition-metal dichalcogenides (TMDs) have attracted significant research interest due to their unique electronic and optical properties [1]. In particular, molybdenum disulfide (MoS_2), with its semiconductor band gap, has been widely studied and proposed for various electronic devices, including photodetectors [2], field effect transistors (FETs) [3, 4], sensors [5], and so on. In addition to monolayer MoS_2, multi-layer MoS_2 has recently been regarded as a promising semiconductor material for nanoelectronics, optoelectronics, and flexible devices [6, 7].

Apart from solely MoS_2-based transistors [3, 4, 8], ultrathin TMD layers could also be combined with other emerging materials for novel heterojunction devices. For example, MoS_2 has been utilized to form p–n diodes with 2D tungsten diselenide (WSe_2) [9] and carbon nanotubes [10]. Recently, 2D MoS_2 films on wide bandgap semiconductor GaN have garnered extensive research efforts to benefit from the unique advantages of both materials [11]. Heterojunction diodes have been successfully demonstrated by transferring a chemical vapor deposition (CVD)-grown MoS_2 layer onto a p-type gallium nitride (p-GaN) surface. However, MoS_2-based devices using micro-mechanical exfoliation [12]

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or layer transfer [11, 13] are not preferred in volume production due to the variation in material size, layer number, and location of transferred MoS_2. It is also believed that the surface states of transferred samples and the residue after the transfer could affect the device performance. Although there have been attempts to directly grow ultrathin MoS_2 layers on GaN, the shape and size of the resulting MoS_2 was limited to be triangular with a maximum side length of several microns [14].

Semiconductor transistors and diodes are key building blocks of functional integrated circuits. So far, there have been reports of MoS_2-based 2D or 2D/3D individual electron devices, however, demonstration of more than one specific type of device is scarce. A platform that is conducive for fabricating both transistors and diodes is uncommon [15], especially a large-area one. In our prior work, large-area continuous MoS_2 films were demonstrated by MoO_3 sulfurization on a SiO_2/Si substrate [16]. In this paper, we report MoS_2-based transistors and diodes fabricated on the same MoS_2/SiO_2/p-GaN/Si platform. Two crucial issues of vertical 2D/3D stack electronics are addressed: (1) CVD growth of wafer-scale MoS_2 on a SiO_2/p-GaN/Si substrate for 2D/3D integration; (2) demonstration of transistors and diodes on the same platform. Specifically, the top-gated MoS_2-based transistors (channel width/length of $\sim 37/6\ \mu$m) show electron mobility of the MoS_2 multi-layer film to be $0.17\ cm^2\ V^{-1}\ s^{-1}$ and an on/off current ratio over 10^5 with distinctive current saturation characteristics. The MoS_2/SiO_2/p-GaN semiconductor/insulator/semiconductor (SIS) heterojunction diodes show good current-rectifying characteristics. The SIS diode could be used as a rectifier or a switch to steer current towards one direction, convert AC into DC voltages or de-modulate AC signals. More importantly, the demonstration of these building block devices on one single platform opens up opportunities for implementing complex nanoscale electronics in the future.

2. Experiment details

The starting sample consists of a magnesium (Mg) doped p-type GaN layer grown on a (111) Si substrate. The sheet resistance of the p-GaN layer was measured to be $\sim 1.93\ \Omega$ cm with a hole mobility of $15.5\ cm^2\ V^{-1}\ s^{-1}$ and hole concentration of $2.0 \times 10^{17}\ cm^{-3}$. Next, a 1 nm thick SiO_2 layer was deposited onto the p-GaN/Si substrates by E-beam evaporation. Then the multi-layer MoS_2 film growth was carried out by CVD at atmospheric pressure in a dual-zone furnace with a 25 mm diameter horizontal quartz tube. Figure 1 schematically shows the MoS_2 multi-layer film structure grown on the SiO_2/p-GaN/Si substrate. The precursor and reactant material were MoO_3 powder (Sigma Aldrich, 99.5%) and sulfur (Sigma Aldrich, 99.5%) respectively. Different from our previous report of growing MoS_2 continuous thin film on SiO_2/Si substrates [16], when growing MoS_2 on the SiO_2/p-GaN substrate, N_2 as the carrier gas and 800 °C growth temperature were used to avoid GaN decomposition. More detailed information about furnace set-up and growth method are provided in the supplementary data section is available online at stacks.iop.org/SST/32/075011/mmedia.

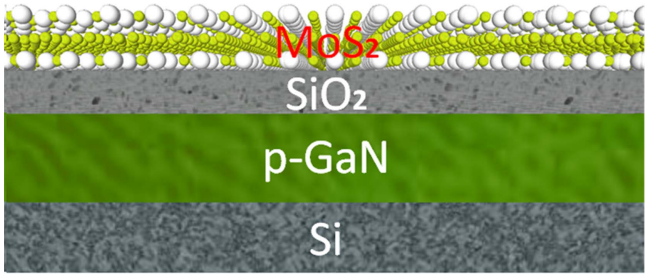

Figure 1. Schematic of the MoS_2 large-area continuous multi-layer film grown on a SiO_2/p-GaN/Si substrate.

Atomic force microscopy (AFM), scanning electron microscopy (SEM), and Raman spectroscopy were used to characterize the surface morphologies of the as-grown MoS_2 multi-layer film. The as-grown MoS_2 continuous multi-layer film was used to fabricate both top-gated FETs and SIS heterojunction diodes using an optical photolithography fabrication process. The metal lift-off process was carefully carried out by immersing the samples in acetone for about one day, cleaning with isopropanol and finished by rinsing and baking on a 110 °C hotplate to avoid SiO_2 or MoS_2 peeling off.

For the top-gate FET fabrication, a 25 nm thick aluminum oxide (Al_2O_3) deposited by thermal atomic layer deposition (ALD) was used as dielectric. The source/drain and gate regions were formed by depositing Ti/Au with thickness of 10/190 nm and 10/90 nm, respectively. For the SIS heterojunction diodes, 50 nm silicon nitride (Si_3N_4) was first deposited on the sample at 200 °C by plasma enhanced chemical vapor deposition (PECVD) using an STS MESC multiplex PECVD. The diode mesa regions were then defined by etching the materials in the unmasked regions using CHF_3/O_2 reactive ion etching. 20/30/80 nm of Pt/Ni/Au was deposited onto the p-GaN layer as p-contact and the sample was annealed in an N_2 ambient at 350 °C for 1 min. The Si_3N_4 layer was then removed by a buffered oxide etch solution after protecting the MoS_2 during annealing. Finally, 10/50 nm of Ni/Au was deposited onto the MoS_2 film as the n-contact.

3. Results and discussion

The microscopic and SEM images of the as-grown MoS_2 samples are displayed in figures 2(a) and (b) respectively. The optical contrast between the MoS_2 continuous multi-layer film and the SiO_2/p-GaN/Si substrate was indicated by scratching the sample with tweezers.

AFM images with $1\ \mu m \times 1\ \mu m$ and $10\ \mu m \times 10\ \mu m$ scanning area of the MoS_2 continuous multi-layer film grown on the SiO_2/p-GaN/Si substrate are shown in figure 3. The $1\ \mu m \times 1\ \mu m$ AFM image, figure 3(a), shows the continuous multi-layer film consists of tiny MoS_2 grains. The root mean square roughness in the $1\ \mu m \times 1\ \mu m$ scan area is 0.91 nm,

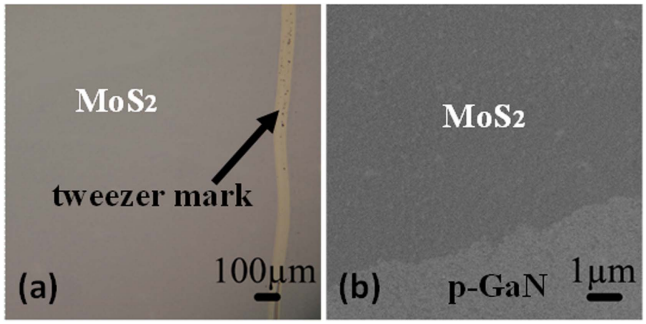

Figure 2. (a) Microscopic and (b) SEM images of MoS_2 large-area continuous multi-layer film with a scratched tweezer mark.

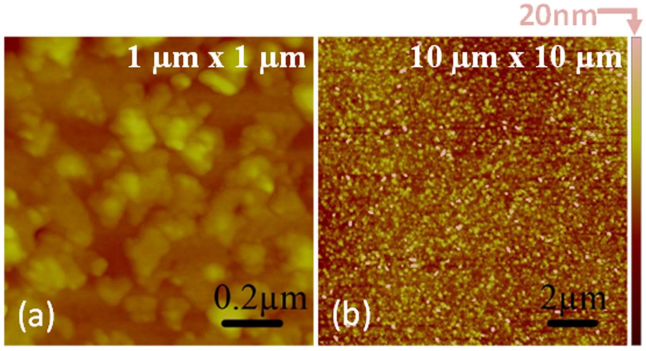

Figure 3. AFM images of the MoS_2 multi-layer film surface with scanning area (a) 1 μm × 1 μm and (b) 10 μm × 10 μm.

which indicates a smooth surface morphology of the MoS_2 continuous multi-layer film.

As there are no innate film edges in the MoS_2 continuous multi-layer film, its thickness cannot be measured directly using AFM. A spectroscopic verification by the Raman spectra was used to obtain the layer number of the MoS_2 nanosheet. Figures 4(a) and (b) showed Raman spectra of samples before and after MoS_2 nanosheet growth. In figure 4(a), with GaN E_2^{high} modes located at 566.51 cm^{-1}, the A_1^{LO} modes located at 733.12 cm^{-1}, and a local vibration mode located at 650.22 cm^{-1}, the measurement results are consistent with those for a Mg-doped GaN layer [17]. Figure 4(b) showed a typical Raman spectra of a sample with MoS_2 grown on top. The E_{2g}^1 modes was located at 382.9 cm^{-1} and the A_{1g} modes at 406.9 cm^{-1}. The spacing between these two peaks was calculated to be 24.0 cm^{-1}, which corresponds to four layers of MoS_2 for the as-grown material. A Raman mapping image of the peak difference between the E_{2g}^1 and A_{1g} modes over an area of 70 μm × 70 μm is displayed in figure 4(c). The mapping image indicated that the peak distance mainly varied between 24.0 and 26.0 cm^{-1}, which implied that over a large area the layer number of the as-grown MoS_2 is uniformly controlled to be 4–5 [18, 19].

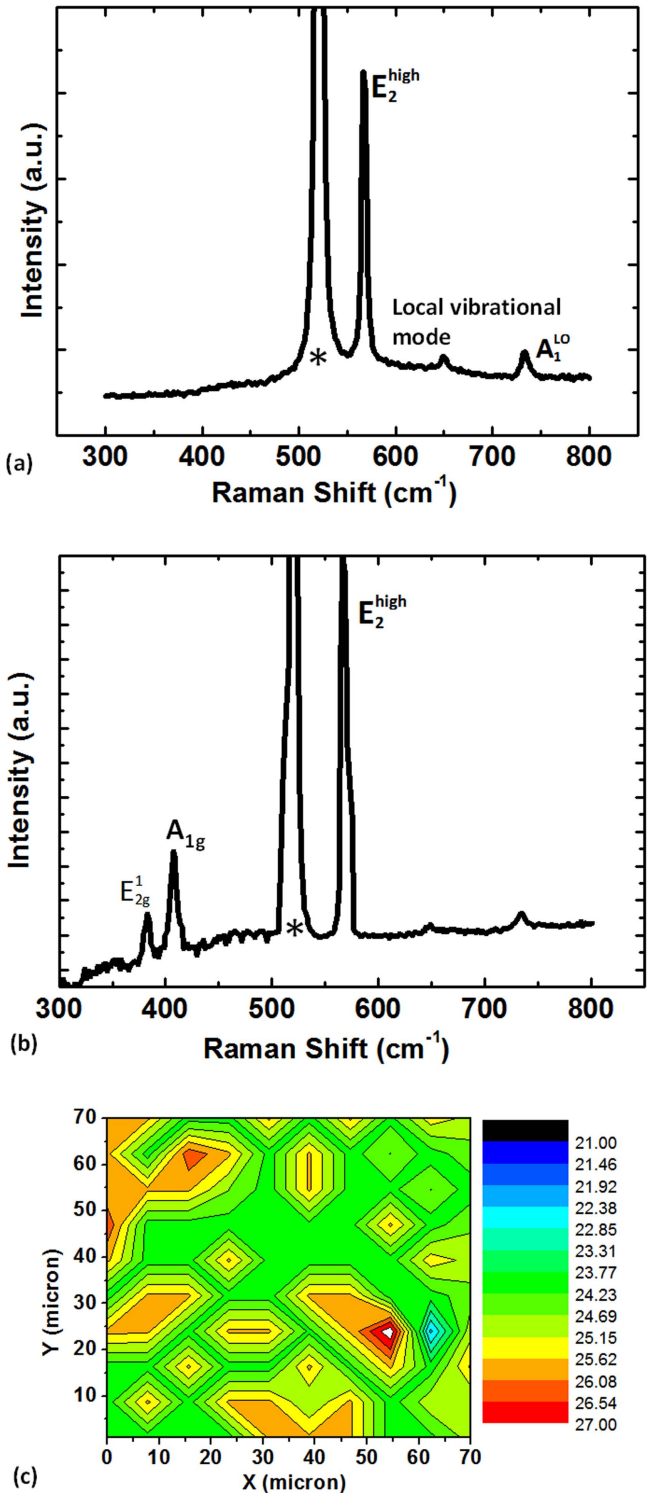

Figure 4. (a), (b) Raman spectra of the SiO_2/p-GaN substrate and the MoS_2/SiO_2/p-GaN sample; * indicates the strong Si signal, which occurs at 520 cm^{-1}; (c) Raman mapping image of E_{2g}^1 and A_{1g} peak spacing over an area of 70 μm × 70 μm.

The schematic cross-sectional structures and an optical image of a top-gate MoS_2 FET are shown in figures 5(a) and (b). The logarithmic scales and linear scales of the DC transfer characteristics (drain current versus gate bias) of the MoS_2 top-gated FETs are shown in figure 5(c). The top gate voltage (V_{gs}) was swept from −2 to +8 V at drain voltages (V_{ds}) of +0.5 to +1.5 V with a step of +0.5 V. The top-gated FETs are depletion-mode n-channel devices which showed an on/off current ratio of 10^5 and a subthreshold swing (SS) of 74 mV dec^{-1}. The SS was extracted at V_{ds} = 1 V and V_{gs}

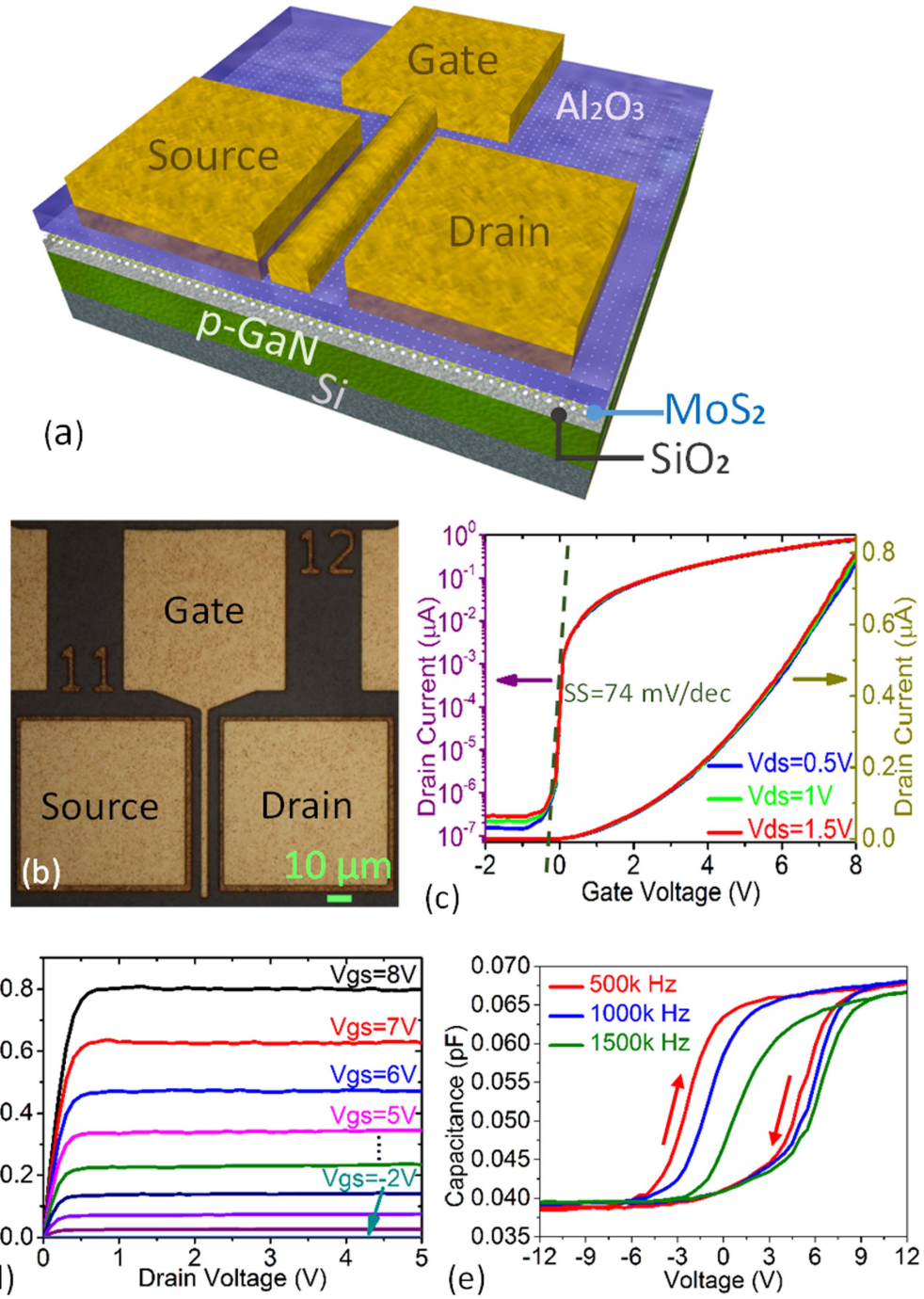

Figure 5. Device structure of MoS_2 top-gated FETs from (a) aerial view and (b) optical microscope view. (c) Logarithmic scale (left) and linear scale (right) of transfer characteristics of the MoS_2 few-layer film. (d) Output curve of the MoS_2 continuous multi-layer film FETs with several top gate voltage biases. (e) Capacitance–voltage measurement of the top-gated FETs at three different frequencies.

slightly lower than 0 V, as shown in figure 5(c). The field effect carrier mobility of the MoS_2 FETs was also extracted by measuring differential resistance [3]: $\mu = (\Delta I_{ds}/\Delta V_g) \times [L/(WC_{ox}V_{ds})]$, where L and W are the channel length and the channel width respectively, C_{ox} is the gate oxide capacitance per unit area, $\Delta I_{ds}/\Delta V_g$ is the slope of the transfer curve taken in the linear region, which is also known as the transconductance, and V_{ds} is the channel bias. As $C_{ox} = 3.54 \times 10^{-3}\,\mathrm{F\,m^{-2}}$ for the 25 nm thick thermal aluminum oxide and $L/W = 6/37\ \mu$m, the calculated field effect carrier mobility of the as-grown MoS_2 continuous multi-layer film FETs was $\sim 0.17\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at $V_{ds} = 0.5$ V. The on/off current ratio and carrier mobility are comparable to the FETs fabricated by MoS_2 thin films on SiO_2/Si substrates which showed carrier mobility ranging from $\sim$0.003 to $\sim 7.23\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [20–24]. It is expected the mobility and on-state current could be greatly improved by optimizing the SiO_2/GaN substrate roughness, MoS_2 nanograin sizes, and also device contacts [3, 4, 6]. Output characteristics of the top-gated MoS_2 FETs was also evaluated by sweeping the V_{ds}

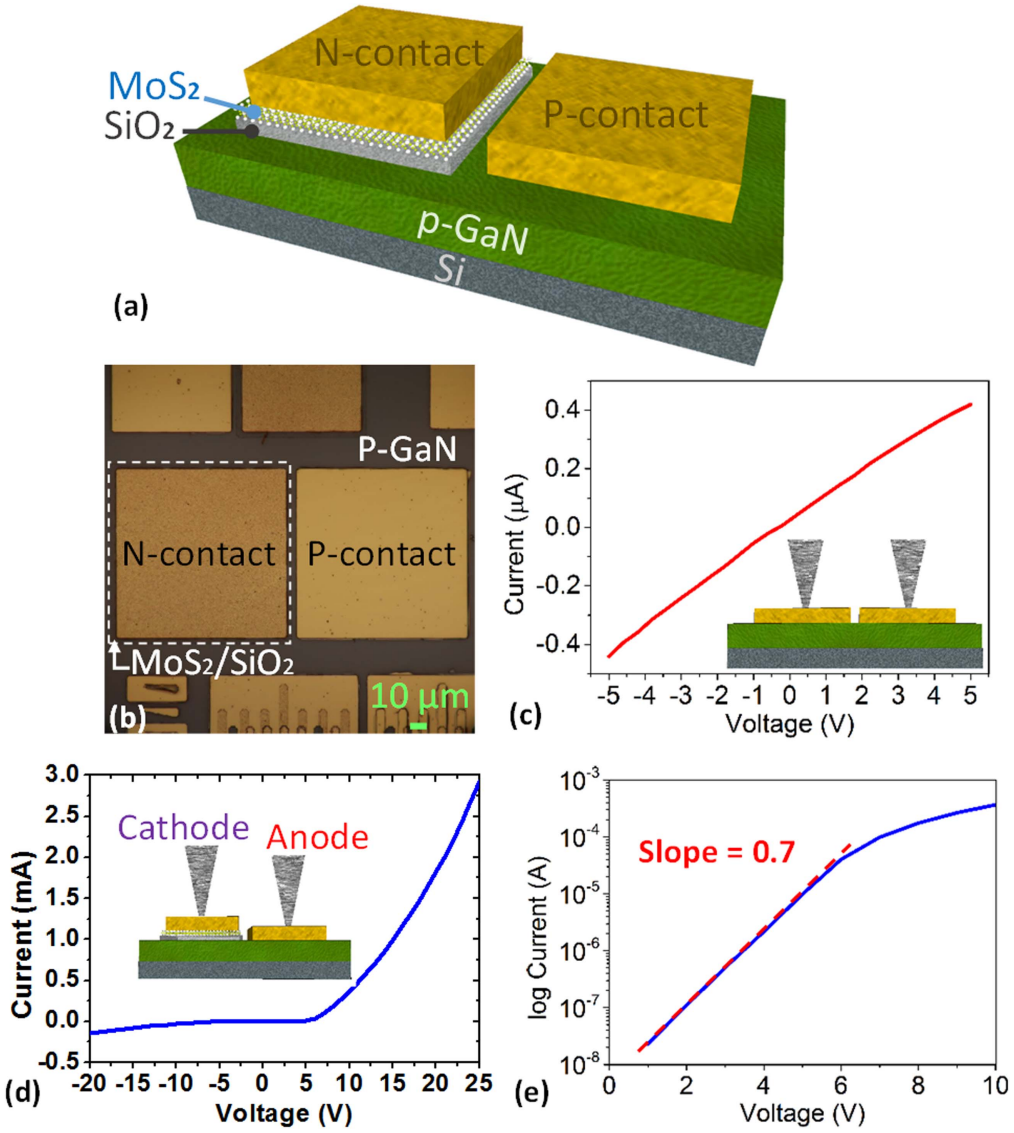

Figure 6. Device structure of MoS_2/SiO_2/p-GaN SIS heterojunction from (a) aerial view and (b) optical microscope view. Current versus bias voltage characteristics of (c) p-GaN-p-GaN contact, (d) SIS heterojunction diode in linear scale, and (e) SIS heterojunction diode in logarithmic scale.

from 0 to +5 V, with gate modulation steps of −1 V from +8 to −2 V, as shown in figure 5(d). For $V_{gs} = +8$ V, the drain current of the device began to saturate with an on-state current of ∼0.8 μA when V_{ds} was only ∼0.7 V. The small on-resistance and early onset of current saturation at a small V_{ds} under various V_{gs} biases has important implication for the device's applications, especially for low operating power electronics.

The quality of the interface between the deposited Al_2O_3 and MoS_2 multi-layer film was also examined by conducting capacitance–voltage (C–V) measurements for the top-gated FETs. While sweeping the top-gate V_{gs} from −12 to +12 V and keeping V_s and V_d grounded, C–V was performed using three frequencies, 500 k Hz, 1 M Hz, and 1.5 M Hz, as shown in figure 5(e). These high-frequency C–V measurements confirm a classic metal-oxide-n-type semiconductor capacitor, as an evident depletion to accumulation transition can be found at negative gate bias. The large magnitude of hysteresis in all three curves points to a conclusion that there is a deficient response of the interface charges between the MoS_2 multi-layer film and Al_2O_3. To explain the large magnitude of the hysteresis, a model, $SS = \frac{kT}{q}\ln 10\left(1 + \frac{C_S}{C_{OX}} + \frac{C_{IT}}{C_{OX}}\right)$, where SS denotes the subthreshold swing, C_S is the semiconductor capacitance, C_{IT} is the interface charge capacitance, C_{OX} is the dielectric capacitance, q is the charge on the electron, k is the Boltzmann's constant, and T is temperature in unit Kelvin, was applied to study the interface charge density. With a SS of 74 mV dec^{-1} obtained by the fitting line shown in the logarithmic scales of the DC transfer characteristics in figure 5(c), the corresponding C_{IT} was calculated to be 8.59×10^{-8} F cm^{-2}, and the density of charge was about 5.36×10^{11} eV^{-1} cm^{-2}, which is comparable to that of MoS_2-based transistors reported in the literature [25, 26]. This may be caused by the yet to be optimized Al_2O_3 grown by ALD at 300 °C [27], resulting in a relatively large hysteresis.

Figures 6(a) and (b) showed the schematic structure and a microscopic image of a processed p-GaN/SiO_2/MoS_2 SIS diode. The typical current–voltage (I–V) curve between the two p-GaN pads is shown in figure 6(c), and the linear I–V relationship reveals an ohmic contact between the Pt/Ni/Au and p-GaN. Figure 6(d) showed the representative I–V curves of the SIS heterojunction diode which had the same p-contact and n-contact area (0.01 mm^2) and inter-pad distance of 5.5 μm. The threshold voltage and series resistance of the diode was extracted to be 5.0 V and 5.3 kΩ. The series resistance was slightly smaller than the SIS tunnel diode made of MoS_2/h-BN/p-GaN [23]. The forward current increased rapidly beyond the threshold voltage and at 25 V, the on-state current was measured to be 2.92 mA, which is translated to a current density of 29 A cm^{-2}. To the best of our knowledge, this current is one of the largest currents reported for the 2D material/GaN vertically-stacked diodes [12, 23], showing the great potential of SIS diodes in this work to be used as a switch. Under reverse bias, the diode showed good current blocking characteristics and the leakage current was measured to be only 30 μA at −10 V. Moreover, no breakdown was observed for reverse voltage up to −25 V. Figure 6(e) shows the logarithmic scale of the SIS diode I–V characteristics. The red dashed line indicates the fitting curve at the small positive bias voltage. Using the ideal diode equation in logarithmic scale, $\log I_D = \frac{q}{nkT}V_D + \log I_S$, where I_D, I_S, and V_D are the diode current, reverse saturation current, and diode voltage respectively, q is the charge on the electron, n is the ideality factor, k is the Boltzmann's constant, and T is temperature in unit Kelvin. With $\frac{kT}{q} = 25.9$ mV at room temperature and from the fitting curve, the ideality factor of the SIS diode was calculated to be 55.2. The large ideality factor in the SIS diode was mainly attributed to a large series resistance induced by the SiO_2 insulator and the p-GaN grown on Si substrates.

In order to qualitatively explain the current flow mechanism of the I–V characteristics at thermal equilibrium, under forward and reverse biases, the band structure of the SIS diode was examined, as shown in figure 7. At thermal equilibrium, the Fermi levels of the MoS_2 and p-GaN are aligned, so the bands of the MoS_2 close to the SiO_2 will bend upward, and the bands of the p-GaN close to the SiO_2 will bend downward. Since the SiO_2 insulating layer obstructs all carriers from passing through the junction, no current will flow through the device. When the device was forward biased, the Fermi level of the MoS_2 will move upward and the bands of the p-GaN close to the SiO_2 will bend upward. This leads to holes accumulating at the SiO_2/p-GaN interface and electrons accumulating at the MoS_2/SiO_2 interface. When above the threshold voltage, the accumulated carriers could tunnel through the thin (1 nm) insulating layer, as schematically shown in figure 7(b). When the SIS diode was reverse biased, the electrons or the holes cannot flow through due to the high potential barrier [13]. Although it is possible for electrons from the p-GaN to tunnel through the thin insulator to the MoS_2 layer, the resultant current is low due to the limited number of electrons in the p-GaN.

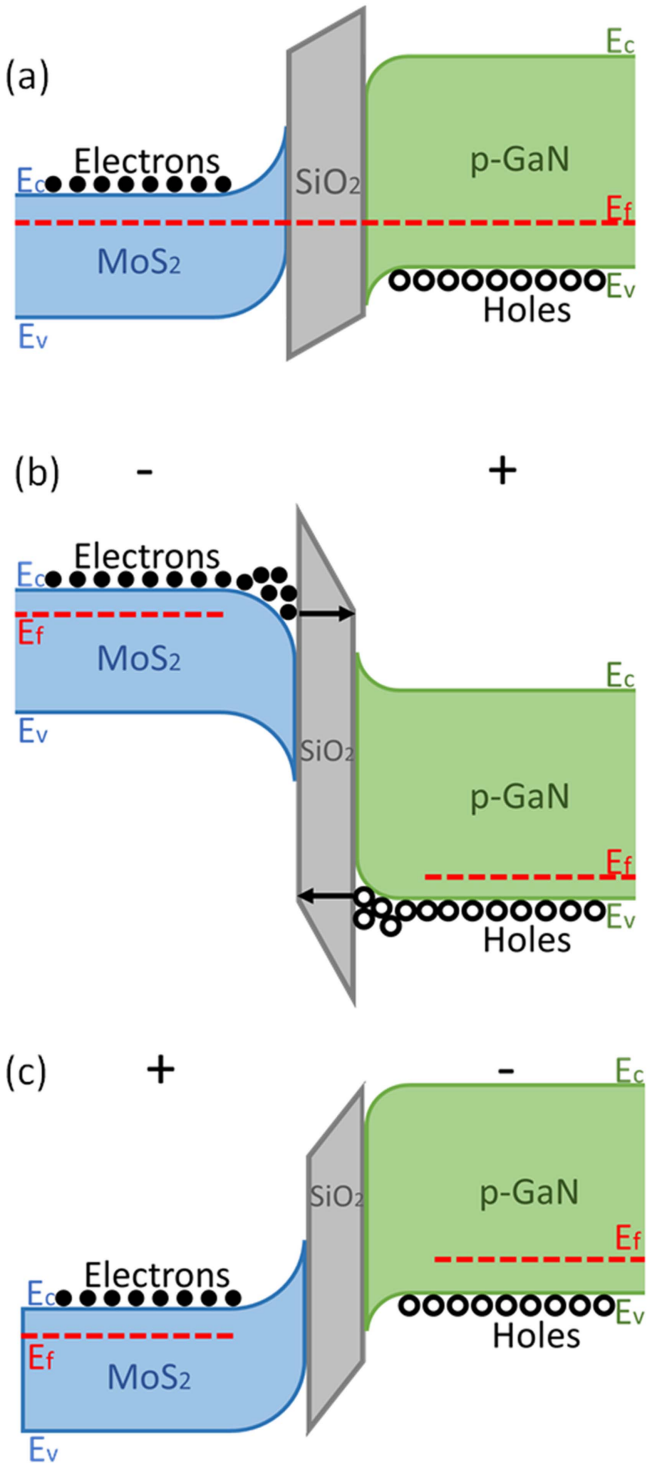

Figure 7. Energy band diagram of the SIS heterojunction diode at thermal equilibrium, under forward bias, and reverse bias.

4. Conclusion

In conclusion, we reported the direct growth of large-area 2D MoS_2 film on a SiO_2/p-GaN/Si substrate for fabrication of MoS_2 top-gated transistors and MoS_2/SiO_2/p-GaN tunnel diodes. The as-grown MoS_2 thin film was characterized by AFM, SEM, and Raman spectroscopy. Fabricated top-gated FETs showed a large on/off current ratio ~10^5, a SS of

74 mV dec^{-1}, carrier mobility of ~0.17 cm^2 V^{-1} s^{-1}, and current saturation over a wide drain voltage range. A vertically stacked SIS heterojunction diode that consists of a few layers of as-grown MoS_2, a thin SiO_2, and p-GaN was also fabricated. The *I–V* characteristics showed a good current rectifying property with a large on-state current of 2.92 mA when the diode is forward biased and small reverse current when reversed-biased. The reported device results suggested great opportunities of implementing electronics using the large area 2D/3D material stacks.

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