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Fully-vertical GaN p-i-n diodes Using GaN-on-Si Epilayers

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***Abstract*— Using GaN-on-Si epilayers, for the first time, fully-vertical p-i-n diodes are demonstrated after Si substrate removal, transfer, and n-electrode formation at the top of the device. After SiO_2 sidewall passivation, the vertical p-i-n diodes, with n-GaN facing up, exhibit a V_{on} of 3.35 V at 1 A/ cm², a low differential on-resistance of 3.3 mΩ cm² at 300 A/cm², and a breakdown voltage of 350 V. The corresponding Baliga's figure of merit (FOM) is 37.0 MW/cm², a very good value for GaN-based p-i-n rectifiers grown on Si substrates. The results indicate that fully-vertical rectifiers using GaN-on-Si epilayers have great potential in achieving cost-effective GaN devices for high-power and high-voltage applications.**

***Index Terms*— GaN-on-Si, p-i-n diodes, rectifiers, power electronics, vertical devices, Si removal.**

I. Introduction

GROUP III nitride materials have been regarded as promising candidates for high power and high frequency devices due to their unique and superior material properties, such as wide energy bandgap, high critical electrical field, and good thermal conductivity [1, 2]. In addition to the conventional lateral structure devices such as AlGaN/GaN HEMTs [3], there has been an increasing research interest in the development of vertical structure GaN transistors and diodes. The advantages of vertical GaN devices include high breakdown voltage in a limited chip area, less impact from thermal issues, and integration flexibility [4-7].

Among GaN-based power devices, p-i-n rectifiers have recently been extensively researched due to their small conduction loss and low reverse leakage current. Currently, the majority of GaN pn junction based rectifiers could be classified into two categories. One is fully-vertical devices based on GaN-on-GaN using homoepitaxial growth [8, 9] or GaN on SiC

The manuscript received March 11, 2016.

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This work was supported by the Research Grants Council (RGC) theme-based research scheme (TRS) of the Hong Kong Special Administrative Region Government under grant T23-612/12-R and the National Natural Science Foundation of China under Grant 51507131.

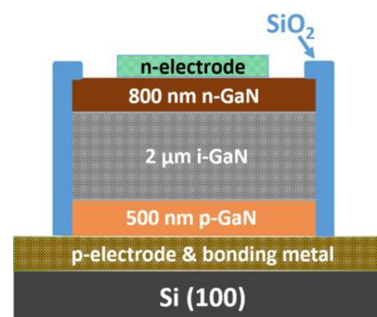

Fig. 1. Schematic cross section of a GaN p-i-n vertical diode on Si through wafer bonding.

using a conductive AlGaN buffer [10]. Rapid progress and excellent performance have been reported for vertical GaN p-i-n diodes grown on n-GaN substrates with the possibility of growing a thick drift layer (20 to 30 µm) and forming electrodes at the top and bottom of the devices. However, expensive and small size low defect density bulk GaN substrates have been an important hurdle in developing GaN fully-vertical power devices and future volume production. The other type is quasi-vertical diodes based on heteroepitaxial growth of GaN layers on lattice-mismatched substrates such as Si, SiC, or sapphire. In this type of structure, the p and n electrodes were formed on the same side of the epilayers after mesa etching to expose p- and n-GaN [11-13]. One main drawback of this design lies in the non-uniform electrical field distribution and current crowding near the mesa edge.

In this letter, we demonstrate, for the first time, a fully-vertical p-i-n diode using GaN-on-Si epilayers. Unlike the traditional quasi-vertical device structure using GaN grown on foreign substrates, the fully-vertical p-i-n diode in this letter was achieved after wafer bonding, Si substrate removal, and n-electrode formation at the top of the device. This device structure combines the advantages of (1) GaN grown on large scale and inexpensive Si substrates, and (2) uniform electrical field and good current spreading. With proper sidewall passivation, we are able to realize fully-vertical p-i-n diodes on Si with a low differential on-resistance ($R_{on,\ diff}$) of 3.3 mΩ cm² at 300 A/cm² and a breakdown voltage of 350 V.

II. Device Structure and Fabrication Process

The GaN p-i-n diodes used in this study were grown on a 6-inch Si (111) substrate by metal organic chemical vapor deposition (MOCVD). The epilayers included a 1.2-µm thick graded AlGaN buffer, an 800-nm thick Si-doped n-GaN layer (~ $n = 2 \times 10^{18}$ cm^{-3}), a 2-µm thick undoped n$^-$-GaN layer (carrier concentration at the order of 10^{16} cm^{-3}), and a 500-nm Mg-doped p-type GaN (~ $p = 2 \times 10^{17}$ cm^{-3}). The full-width at

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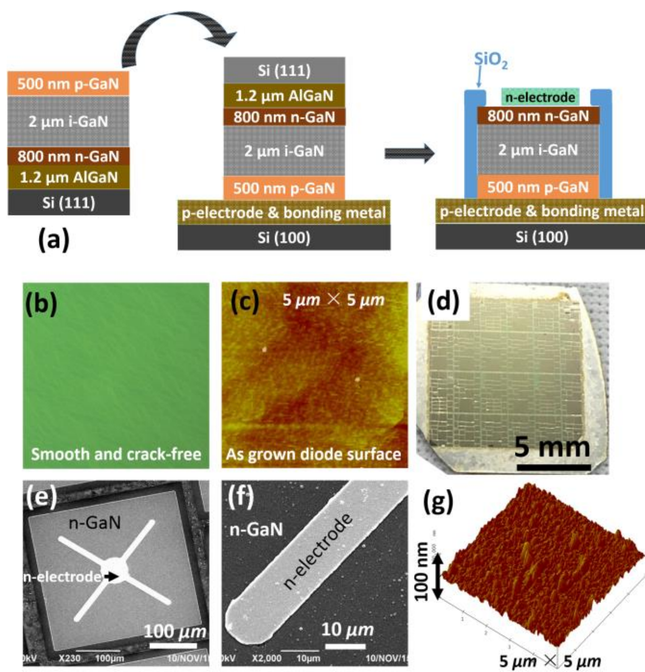

Fig. 2. (a) Main steps in fabricating vertical pin diodes on Si; (b, c) As grown pin diode surface characterized by optical microscopy and AFM; (d) An image of pin epilayers bonded onto Si (100); (e, f) SEM images of a fabricated pin diode on Si with n-GaN facing up; (g) AFM image of n-GaN surface after AlGaN buffer removal.

half-maximum (FWHM) of the X-ray diffraction rocking curves were 351 arcsec and 540 arcsec for (002) and (102) orientations, respectively. The total dislocation density was estimated to be 9×10^8 cm^{-2} through empirical calculation.

The process steps of fully-vertical p-i-n diodes on the Si (100) carrier are briefly described as follows [Fig.2 (a)]: individual p-i-n diodes were first isolated by etching the epilayers in trenches down to the Si (111) growth substrate using inductively coupled plasma (ICP). 5 nm/5nm Ni/Au metal bilayers were deposited on the p-GaN and annealed in 4:1 N_2-O_2 mixture at 570 ℃ for ohmic contact formation. Then the wafer was bonded to a Si (100) carrier through Cu-Sn-Cu metal bonding at 280 ℃ for 30 seconds to minimize thermal degradation of the p-type contact. The original Si (111) growth substrate was removed by mechanical grinding and ICP etching. As shown in Fig. 2 (d), very high transfer yield of the GaN epilayer was achieved as almost all the devices were flip-bonded onto the Si carrier except for a few devices at the edges. Afterward, the sidewalls of the p-i-n diodes were passivated by depositing a layer of SiO_2 using plasma enhanced chemical vapor deposition (PECVD). Finally, the AlGaN buffer was removed and Cr/Au-based metal stack was deposited on the exposed n-GaN layer as n-electrode.

III. Results and discussion

Fig.2 (b-g) shows images of the as-grown and processed vertical p-i-n diode surfaces. The optical and atomic force microscopy (AFM) images of the as-grown GaN-on-Si (111) epilayers show a smooth and crack-free surface for process. The root mean square (rms) roughness across a 5 $\mu m \times 5$ μm scanned area was only 0.55 nm. After flip-chip wafer bonding and growth substrate removal, the insulating AlGaN buffer was eliminated by a mixture gas of BCl_3/Cl_2/He to keep an uniform etching rate and to guarantee a relatively smooth n-GaN surface for n-metal deposition, as shown in Fig.2 (e, f, g). The rms roughness of exposed n-GaN surface was measured to be 4.96 nm over a 5 $\mu m \times 5$ μm scanned area. The reason to take surface roughness into account is that a rough surface would significantly increase leakage current due to larger local electrical field at the surface peak [14].

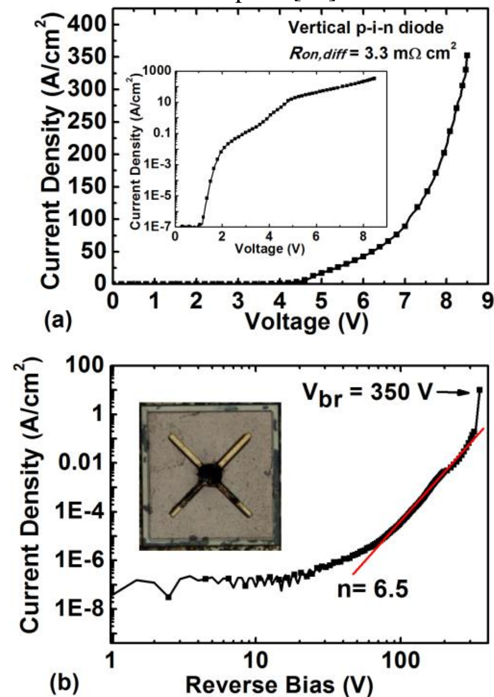

Fig. 3. Forward and reverse I-V characteristics of vertical p-i-n diodes; (Inset in (b)) an image of destroyed pin diode surface after breakdown.

Fig. 3 (a) shows the forward I-V characteristics of a finished 0.11 mm^2 GaN vertical p-i-n diode. The V_{on}, extracted at the current density of 1 A/cm^2, was 3.35 V, which is close to the bandgap of GaN. It can be found that the resistance was large under low forward bias due to the resistive drift region. As the bias was increased, holes and electrons were injected into the drift region, leading to a reduction of resistance. The differential on-resistance ($R_{on,\,diff}$) of the processed diode on Si was 3.3 mΩ cm^2 at 300 A/cm^2 and the corresponding voltage drop was 8.38 V. The calculated voltage drop across the i-GaN drift layer using an analytical model [15] was around 1.3 V, indicating a large portion of the voltage drop was associated with the contact resistance to and series-resistance of the p-GaN itself. Good current spreading through the bonding metal have helped mitigate current crowding [16] which is often observed in the quasi-vertical device structures. The on-resistance and voltage drop can be further reduced by growing p-GaN layer with higher mobility and optimized ohmic contact metal scheme. Fig.3 (b) displays the reverse I-V characteristics of the GaN vertical p-i-n diode. At -200V, the typical reverse current density of the vertical p-i-n diode was measured to be 1×10^{-2} A/cm^2, which was comparable to GaN p-i-n diodes fabricated on original foreign substrates [12, 13, 17]. The results indicated that the Si removal and epilayer transfer process did not

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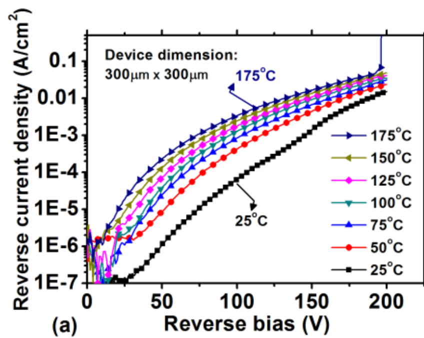
degrade the current blocking capability after proper sidewall passivation. The reverse leakage current could be further suppressed by applying some edge termination technologies, such as sidewall treatment and additional proper passivation material. [18] As shown in Fig.3 (b), a breakdown voltage of 350 V was obtained and the reverse current before breakdown could be modeled by a space-charge-limited current (SCLC) conduction [19], where the reverse current was proportional to V^n and n was calculated to be 6.5 by fitting. According to Zhou's model, both acceptor traps and donor traps exist in the GaN layer grown on Si. In our diode, when the reverse voltage was larger than 40 V, acceptor traps have been fully ionized and donor traps started to get neutralized. As the Fermi level kept moving towards the conduction band, more free electrons were generated in the conduction band, leading to a rapid increase of reverse current.

Fig. 4 (a) shows the reverse I-V characteristics of a 300 μm × 300 μm vertical p-i-n diode at different temperatures from 25 ℃ to 175 ℃. The reverse current increase with the temperature is believed to be associated with thermally generated carriers and enhanced carrier hopping through dislocations or traps [20]. At -30 V, the thermal activation energy was extracted to be 105 meV from the log (J) – 1/T plot. The thermal activation energy (105 meV) suggested existence of deep hopping centers, through which electrons were excited to the conduction band in the depletion region [21].As shown in Fig. 4(a), at high temperature and high reverse bias, it was believed that two leakage mechanisms, SCLC conduction and carrier hopping, co-existed that the leakage current increased rapidly[22]. As a result, it was also observed that the reverse breakdown voltage decreased at higher temperatures. The fabricated 300 μm square p-i-n diode showed a breakdown voltage of 197 V at an elevated temperature of 175 ℃.



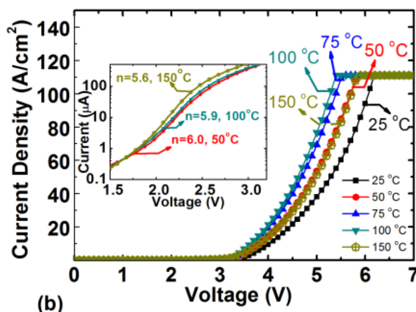


Fig. 4. (a) Reverse I-V characteristics of a vertical pin diode on Si at different temperatures; (b) Forward I-V characteristics of a vertical diode at different temperatures.

Fig.4 (b) shows the forward I-V characteristics of the vertical diode at different temperatures. As the operating temperature was elevated, the diode showed slightly improved ideality factor from 6.0 at 50 ℃ to 5.6 at 150 ℃ as a result of improved dopant ionization in the p-GaN. The forward voltage at 100 A/cm^2 was gradually decreased from 6.02 V at 25 ℃ to 5.28 V at 100 ℃. When the temperature was raised to higher than 100 ℃, the forward voltage at 100 A/cm^2 started to increase, e.g., 5.72 V at 150 ℃, which was attributed to degraded p-type contact resistance after continuous thermal stress [23] and potential metal diffusion from bonding metals, considering the very thin ohmic contact metal scheme.

The performance of our fully-vertical diodes was also benchmarked in a figure of merit (FOM) plot shown in Fig. 5 [8-13, 17, 24-30]. The small differential on-resistance of 3.3 mΩ-cm^2 demonstrated in this work was attributed to conductivity modulation from carrier injection and excellent current spreading in the fully-vertical structure. Combining the measured breakdown voltage of 350 V and on-state forward resistance, the Baliga's FOM is calculated to be 37.0 MW/cm^2 for a 0.11 mm^2 diode. To our knowledge, this is the best-reported data for GaN p-i-n rectifiers grown on Si substrates. Considering the simple active GaN epi-layers with a drift region of only 2 μm that can be grown on large area Si substrates, the methods reported here showed great potential in achieving cost-effective GaN vertical devices for high-power and high-voltage switching applications.

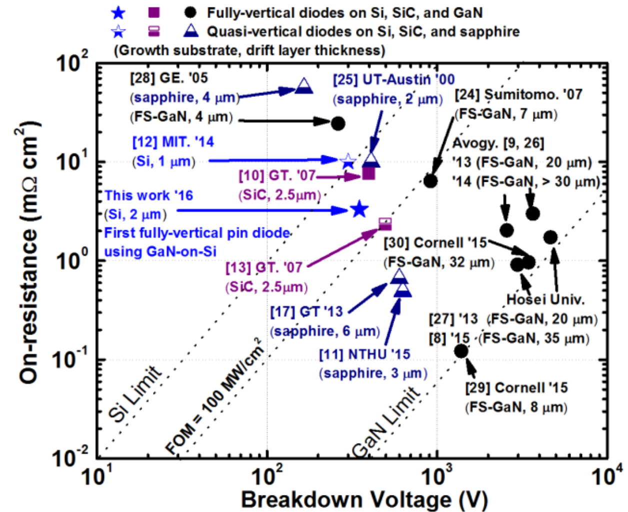


Fig. 5. Relationship between the specific on-resistance and breakdown voltage of GaN vertical p-i-n rectifiers on various substrates.

IV. CONCLUSIONS

For the first time, we demonstrated fully-vertical p-i-n diodes using GaN-on-Si epilayers after a simple substrate transfer process. The superior device performance including low differential on-resistance of 3.3 mΩ cm^2 at 300 A/cm^2 and a breakdown voltage of 350 V leading to a Baliga's FOM of 37.0 MW/cm^2, is the highest for GaN p-i-n diode grown on Si. The p-i-n diode fabrication method reported here together with GaN epilayers grown on large scale Si substrates paved a promising path for achieving cost-effective high-power switching devices.

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REFERENCES

[1] U. K. Mishra, L. Shen, T. E. Kazior, and Y. F. Wu, "GaN-based RF power devices and amplifiers," *Proceedings of the IEEE,* vol. 96, pp. 287-305, 4414367, 2008. DOI: 10.1109/JPROC.2007.911060

[2] S. J. Pearton and F. Ren, "GaN electronics," *Advanced Materials,* vol. 12, pp. 1571-1580, 2000. DOI: 10.1002/1521-4095(200011)12:21<1571::AID-ADMA1571>3.0.CO;2-T

[3] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Misha, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Transactions on Electron Devices,* vol. 48, pp. 560-566, 2001. DOI: 10.1109/16.906451

[4] S. Chowdhury and U. K. Mishra, "Lateral and vertical transistors using the AlGaN/GaN Heterostructure," *IEEE Transactions on Electron Devices,* vol. 60, pp. 3060-3066, 6605590, 2013. DOI: 10.1109/TED.2013.2277893

[5] T. Uesugi and T. Kachi, "Which are the Future GaN Power Devices for Automotive Applications, Lateral Structures or Vertical Structures?," *2011 CS MANTECH Technical Digest,* pp. 1-4, May 2011.

[6] T. D. Heidel, D. Henshall, and P. Gradzki, "Strategies for Wide Bandgap, Inexpensive Transistors for Controlling High-Efficiency Systems," *2015 CS MANTECH Technical Digest,* pp. 1-4.

[7] Y. Zhang, M. Sun, Z. Liu, D. Piedra, H. S. Lee, F. Gao, T. Fujishima, and T. Palacios, "Electrothermal simulation and thermal performance study of GaN vertical and lateral power transistors," *IEEE Transactions on Electron Devices,* vol. 60, pp. 2224-2230, 6522859, 2013. DOI: 10.1109/TED.2013.2261072

[8] H. Ohta, N. Kaneda, F. Horikiri, Y. Narita, T. Yoshida, T. Mishima, and T. Nakamura, "Vertical GaN p-n Junction Diodes With High Breakdown Voltages Over 4 kV," *Electron Device Letters, IEEE,* vol. 36, pp. 1180-1182, 2015. DOI: 10.1109/LED.2015.2478907

[9] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Bour, T. Prunty, and D. Disney, "3.7 kV vertical GaN PN diodes," *IEEE Electron Device Letters,* vol. 35, pp. 247-249, 6684571, 2014. DOI: 10.1109/LED.2013.2294175

[10] D. Yoo, J. Limb, J.-H. Ryou, W. Lee, and R. Dupuis, "Epitaxial Growth and Device Design Optimization of Full-Vertical GaN p-i-n Rectifiers," *Journal of Electronic Materials,* vol. 36, pp. 353-358, 2007. DOI: 10.1007/s11664-006-0069-1

[11] B. S. Zheng, P. Y. Chen, C. J. Yu, Y. F. Chang, C. L. Ho, M. C. Wu, and K. C. Hsieh, "Suppression of current leakage along mesa surfaces in GaN-based p-i-n diodes," *IEEE Electron Device Letters,* vol. 36, pp. 932-934, 7163548, 2015. DOI: 10.1109/LED.2015.2458899

[12] Y. Zhang, M. Sun, D. Piedra, M. Azize, X. Zhang, T. Fujishima, and T. Palacios, "GaN-on-Si vertical schottky and p-n diodes," *IEEE Electron Device Letters,* vol. 35, pp. 618-620, 6786327, 2014. DOI: 10.1109/LED.2014.2314637

[13] J. B. Limb, D. Yoo, J. H. Ryou, S. C. Shen, and R. D. Dupuis, "Low on-resistance GaN pin rectifiers grown on 6H-SiC substrates," *Electronics Letters,* vol. 43, pp. 366-367, 2007. DOI: 10.1049/el:20070065

[14] Y. P. Zhao, G. C. Wang, T. M. Lu, G. Palasantzas, and J. T. M. De Hosson, "Surface-roughness effect on capacitance and leakage current of an insulating film," *Physical Review B,* vol. 60, pp. 9157-9164, 1999. DOI: 10.1103/PhysRevB.60.9157

[15] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*: Springer US, 2010.pp.203-277. DOI:10.1007/978-0-387-47314-7

[16] L. Chi-Kang and W. Yuh-Renn, "Study on the Current Spreading Effect and Light Extraction Enhancement of Vertical GaN/InGaN LEDs," *Electron Devices, IEEE Transactions on,* vol. 59, pp. 400-407, 2012. DOI: 10.1109/TED.2011.2176132

[17] T. T. Kao, J. Kim, Y. C. Lee, M. H. Ji, T. Detchprohm, R. D. Dupuis, and S. C. Shen, "Homojunction GaN p-i-n rectifiers with ultra-low-on-state resistance," in *CS MANTECH 2014 - 2014 International Conference on Compound Semiconductor Manufacturing Technology*, 2014, pp. 157-160.

[18] Y. Zhang, M. Sun, H. Y. Wong, Y. Lin, P. Srivastava, C. Hatem, M. Azize, D. Piedra, L. Yu, T. Sumitomo, N. De Almeida Braga, R. V. Mickevicius, and T. Palacios, "Origin and Control of OFF-State Leakage Current in GaN-on-Si Vertical Diodes," *IEEE Transactions on Electron Devices,* vol. 62, pp. 2155-2161, 7105900, 2015. DOI: 10.1109/TED.2015.2426711

[19] C. Zhou, Q. Jiang, S. Huang, and K. J. Chen, "Vertical leakage/breakdown mechanisms in AlGaN/GaN-on-Si devices," *IEEE Electron Device Letters,* vol. 33, pp. 1132-1134, 6232436, 2012. DOI: 10.1109/LED.2012.2200874

[20] E. J. Miller, E. T. Yu, P. Waltereit, and J. S. Speck, "Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular-beam epitaxy," *Applied Physics Letters,* vol. 84, pp. 535-537, 2004. DOI:http://dx.doi.org/10.1063/1.1644029

[21] Q. Shan, D. S. Meyaard, Q. Dai, J. Cho, E. Fred Schubert, J. Kon Son, and C. Sone, "Transport-mechanism analysis of the reverse leakage current in GaInN light-emitting diodes," *Applied Physics Letters,* vol. 99, p. 253506, 2011. DOI: http://dx.doi.org/10.1063/1.3668104

[22] Y. Zhang, H. Y. Wong, M. Sun, S. Joglekar, L. Yu, N. A. Braga, R. V. Mickevicius, and T. Palacios, "Design space and origin of off-state leakage in GaN vertical power diodes," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, pp. 35.1.1-35.1.4.DOI: 10.1109/IEDM.2015.7409830

[23] M. Meneghini, L. R. Trevisanello, U. Zehnder, G. Meneghesso, and E. Zanoni, "Reversible Degradation of Ohmic Contacts on p-GaN for Application in High-Brightness LEDs," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 3245-3251, 2007. DOI: 10.1109/TED.2007.908900

[24] Y. Yoshizumi, S. Hashimoto, T. Tanabe, and M. Kiyama, "High-breakdown-voltage pn-junction diodes on GaN substrates," *Journal of Crystal Growth,* vol. 298, pp. 875-878, 2007. DOI: 10.1016/j.jcrysgro.2006.10.246

[25] T. G. Zhu, D. J. H. Lambert, B. S. Shelton, M. M. Wong, U. Chowdhury, H. K. Kwon, and R. D. Dupuis, "High-voltage GaN pin vertical rectifiers with 2 μm thick i-layer," *Electronics Letters,* vol. 36, pp. 1971-1972, 2000. DOI: 10.1049/el:20001329

[26] I. C. Kizilyalli, T. Prunty, and O. Aktas, "4-kV and 2.8-mohm cm^2 Vertical GaN p-n Diodes With Low Leakage Currents," *Electron Device Letters, IEEE,* vol. 36, pp. 1073-1075, 2015. DOI: 10.1109/LED.2015.2474817

[27] Y. Hatakeyama, K. Nomoto, A. Terano, N. Kaneda, T. Tsuchiya, T. Mishima, and T. Nakamura, "High-breakdown-voltage and low-specific-on-resistance gan p-n junction diodes on free-standing gan substrates fabricated through low-damage field-plate process," *Japanese Journal of Applied Physics,* vol. 52, 028007, 2013. DOI: 10.7567/JJAP.52.028007

[28] X. A. Cao, H. Lu, S. F. Leboeuf, C. Cowen, S. D. Arthur, and W. Wang, "Growth and characterization of GaN PiN rectifiers on free-standing GaN," *Applied Physics Letters,* vol. 87, 053503, 2005. DOI: 10.1063/1.2001738

[29] Z. Hu, K. Nomoto, B. Song, M. Zhu, M. Qi, M. Pan, X. Gao, V. Protasenko, D. Jena, and H. G. Xing, "Near unity ideality factor and Shockley-Read-Hall lifetime in GaN-on-GaN p-n diodes with avalanche breakdown," *Applied Physics Letters,* vol. 107, p. 243501, 2015. DOI: http://dx.doi.org/10.1063/1.4937436

[30] K. Nomoto, Z. Hu, B. Song, M. Zhu, M. Qi, R. Yan, V. Protasenko, E. Imhoff, J. Kuo, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, "GaN-on-GaN p-n power diodes with 3.48 kV and 0.95 $m\Omega\text{-}cm^2$: A record high figure-of-merit of 12.8 GW/cm^2," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, pp. 9.7.1-9.7.4. DOI: 10.1109/IEDM.2015.7409665

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