Growth and characterization of horizontal GaN wires on silicon

Xinbo Zou, Xing Lu, Ryan Lucas, Thomas F. Kuech, Jonathan W. Choi, Padma Gopalan, and Kei May Lau

Citation: Applied Physics Letters **104**, 262101 (2014); doi: 10.1063/1.4886126
View online: http://dx.doi.org/10.1063/1.4886126
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/104/26?ver=pdfcov
Published by the AIP Publishing

Growth and characterization of horizontal GaN wires on silicon

Xinbo Zou,[1,2] Xing Lu,[1] Ryan Lucas,[3] Thomas F. Kuech,[2,3] Jonathan W. Choi,[4] Padma Gopalan,[4] and Kei May Lau[1,2,a)]
[1]*Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Kowloon, Hong Kong*
[2]*HKUST Jockey Club Institute for Advanced Study, The Hong Kong University of Science and Technology, Kowloon, Hong Kong*
[3]*Department of Chemical and Biological Engineering, University of Wisconsin-Madison, Madison, Wisconsin 53706, USA*
[4]*Department of Materials Science and Engineering, University of Wisconsin-Madison, Madison, Wisconsin 53706, USA*

(Received 13 April 2014; accepted 18 June 2014; published online 30 June 2014)

We report the growth of in-plane GaN wires on silicon by metalorganic chemical vapor deposition. Triangular-shaped GaN microwires with semi-polar sidewalls are observed to grow on top of a GaN/Si template patterned with nano-porous SiO_2. With a length-to-thickness ratio ~200, the GaN wires are well aligned along the three equivalent $\langle 11\bar{2}0 \rangle$ directions. Micro-Raman measurements indicate negligible stress and a low defect density inside the wires. Stacking faults were found to be the only defect type in the GaN wire by cross-sectional transmission electron microscopy. The GaN wires exhibited high conductivity, and the resistivity was 20–30 mΩ cm, regardless of the wire thickness. With proper heterostructure and doping design, these highly aligned GaN wires are promising for photonic and electronic applications monolithically integrated on silicon. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4886126]

III-nitride wires of nanometer to micrometer scales have gained extensive research interest due to their potential applications in novel photonic and electronic devices including light-emitting diodes (LEDs),[1,2] lasers,[3] transistors,[4] and so on. In particular, GaN microwires are drawing increasing attention as building blocks such as natural microcavity[5] and waveguide[6] in constructing optoelectronic devices due to their good crystalline quality, smooth surface, and negligible propagation loss. In addition, the micrometer scale of the wires enables using inexpensive ultraviolet photolithography for fabrication.

In the past decade, great emphasis has been put on the synthesis of vertical or out-of-plane GaN wires. Catalyst-assisted growth of GaN wires has been demonstrated by vapor-liquid-solid (VLS) growth,[7] molecular beam epitaxy (MBE),[8] metalorganic chemical vapor deposition (MOCVD),[9] and selective growth using an anodic alumina template.[10] However, metal catalysts inevitably lead to residual contamination within the semiconductor wires.[11] Besides these bottom-up methods, GaN wires have also been achieved by direct top-down dry etching process.[12] Despite all kinds of growth methods, vertical or out-of-plane GaN wires are the dominating type since wurtzite GaN possesses a preferred [0001] growth direction.[13]

While there are many studies of out-of-plane wires, comparatively few studies have been devoted to the growth and fabrication of horizontal GaN wire structures.[14–17] As a result, their material properties and potential for device fabrication are yet to be fully studied and exploited. Being compatible with planar device processing technology, in-plane GaN wires could be more easily integrated with modern electronic device fabrication processes.[18] Horizontal wires would have no need for post-growth transfer onto a new host substrate and could be *in-situ* processed without losing control of their crystallographic orientations. Fabrication of large-scale array-based devices utilizing well-aligned GaN wires is therefore possible. Hence, a thorough study of the growth and material properties of horizontal GaN nano- or micro-wires is highly desirable.

In this Letter, we report the growth of catalyst-free in-plane GaN microwires on silicon by MOCVD. A thin GaN buffer layer was first deposited on a bare (111) Si substrate and patterned with a nano-porous SiO_2 mask. GaN wires with lengths up to millimeter scale were then grown on this porous template. Interestingly, GaN wires are observed to nucleate on crack lines originating from the thermal mismatch between the GaN buffer and silicon substrate. As a result, GaN wires are grown along the three equivalent $\langle 11\bar{2}0 \rangle$ directions. Notably, the initially grown nanowire length and thickness scale with growth time, thus enabling flexibility in device structure design. The GaN microwires possess a low defect density with only a few stacking faults (SFs) observed within the wurtzite phase wire structure. Electrical measurement reveals that the GaN microwires exhibit high conductivity and that the resistivity is independent of wire thickness. With proper heterostructure design, the nitride-based wires can potentially be used for optoelectronics or high-speed transistor applications.

The GaN wires were grown on a nano-patterned GaN/Si template in an AIXTRON2000HT MOCVD system. The growth structure is schematically illustrated in Fig. 1(a). A 30-nm thick AlN was first deposited on a 2-in. (111) Si substrate as the nucleation layer, followed by a 250-nm thick GaN buffer.[19] Next, a 20-nm thick SiO_2 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) and annealed at the temperature used for subsequent

a)Electronic mail: eekmlau@ust.hk

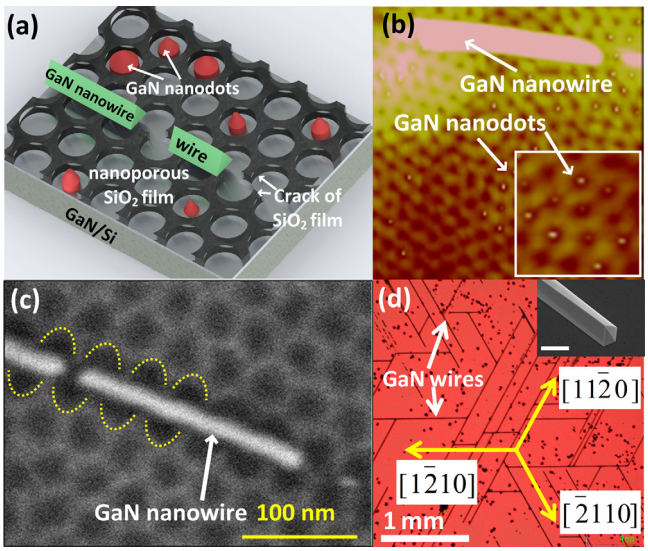

FIG. 1. (a) Schematic of GaN regrowth on the nanoscale porous SiO_2/GaN/Si template; (b) AFM image (550 nm × 550 nm) showing coexistence of GaN nanodots and nanowire on the nanoporous SiO_2 template, inset: a zoomed-in graph with GaN nanodots; (c) SEM image of a GaN nanowire grown on a crack-line in the oxide mask (note a split and shift of SiO_2 nanoholes in the GaN nucleation region; the rim of cracked SiO_2 mask outlined with dotted lines); (d) OM images of 10 μm-thick GaN wires along the three equivalent $\langle 11\bar{2}0\rangle$ directions (scale of inset SEM image: 10 μm).

'regrowth.' A cylinder-forming diblock copolymer film of poly(styrene-*block*-methyl methacrylate) (PS-*b*-PMMA) (Polymer Source Inc., molecular weight (MW): 46 kg/mol for PS and 21 kg/mol for PMMA, polydispersity index (PDI): 1.09) was spin-coated and thermally annealed on the wafer surface after a brush layer pretreatment.[20] After annealing, the self-assembled, vertically oriented PMMA cylinders were selectively removed by ultraviolet irradiation and acetic acid. Subsequently, the left-behind nanohole patterned PS mask was transferred to the underlying SiO_2 layer by dilute hydrofluoric acid.[21] A high density ($\sim 6.3 \times 10^{10}$ cm^{-2}) array of nanoholes were observed in the SiO_2 layer with the average hole diameter and pitch size of 22 and 40 nm, respectively. GaN wire growth was then performed on this porous template. Trimethylgallium (TMGa) and ammonia were employed as gallium and nitrogen precursors for GaN regrowth. The regrowth temperature and initial V/III ratio were 1080 °C and 12 000, respectively. After growth, we examined the GaN wires by optical microscope (OM), scanning electron microscope (SEM), and atomic force microscope (AFM). Stress status and crystal quality were assessed by micro-Raman spectroscopy. Cross-sectional transmission electron microscopy (TEM) was employed to investigate the structural properties of GaN wires. To evaluate the potential for these wires to be used as electrical devices, we fabricate electrodes and measure the electrical conductivity of GaN wires.

The use of nano-porous SiO_2 mask is the key for GaN nano- or micro- wire nucleation. As shown in Figs. 1(b) and 1(c), the nano-openings formed in the SiO_2 layer were uniformly distributed on the wafer surface. GaN nanodots were found to form in some of the openings, as labeled in the AFM image and the inset of Fig. 1(b). The GaN nanodots were confined to selectively grow inside the SiO_2 nano-openings[22] where the underlying GaN was exposed. The nucleation of GaN wires, on the other hand, appears to occur by a different mechanism. It is found that the wires consistently grew along the three equivalent $\langle 11\bar{2}0\rangle$ directions associated with the underlying GaN buffer, as displayed in Fig. 1(d). Moreover, we observed that the GaN wires always nucleate at cracks in the SiO_2 masking layer (see the separation and shift of SiO_2 nanoholes in Fig. 1(c)). These crack lines in the nanoporous oxide film align to the aforementioned crystalline directions of GaN. It is well known that GaN epitaxially grown on silicon tends to crack along $\langle 11\bar{2}0\rangle$ to release the thermally derived tensile stress. These cracks appear to propagate up to and through the nanoporous SiO_2 mask layer during the template preparation process. The subsequently exposed GaN buffer at this narrow crack became the nucleation site for the wire growth. With further optimizations in the growth and patterning conditions, arrays of high-density and well-aligned GaN wires can potentially be synthesized for various device applications.

The initially grown GaN nanowires are typically tens of nanometers in width and hundreds of nanometers in length, although the overgrown in-plane GaN wires can evolve to much larger dimensions. Fig. 2(a) shows an array of parallel GaN wires with thickness of ~1 μm and tens to several hundred micrometers in length. In particular, a six-minute growth can yield GaN wires with thickness ~1 μm at a low TMGa flow of 22 μmol/min. The growth rate along [0001] direction in GaN wire is significantly faster compared with a planar film growth rate (~5 nm/min) using the same growth parameters. At longer growth times, the overall size of GaN wires increases, and a 10-μm thick wire can reach 1–2 mm in length [Fig. 1(d)]. This indicates a fast growth rate along the three equivalent $[11\bar{2}0]$ directions in addition to [0001] direction. Interestingly, the size and density of GaN nanodots did not increase. There is a possible growth competition between

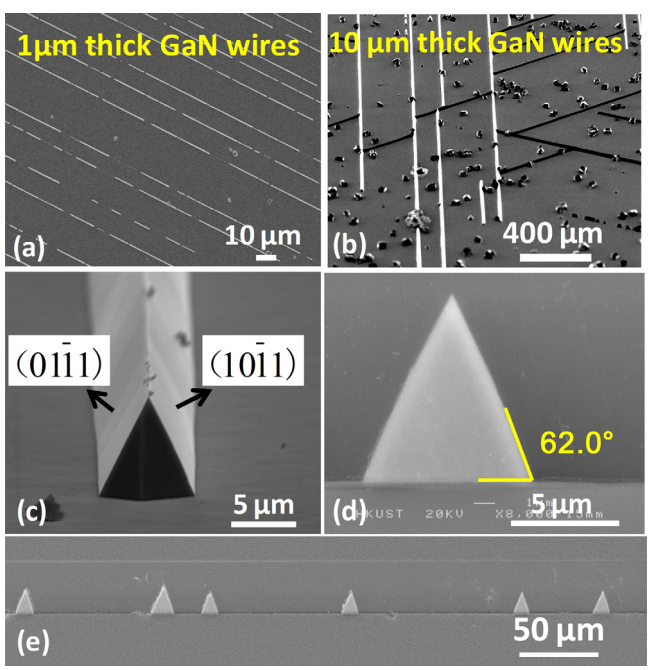

FIG. 2. (a) Plan-view SEM image of parallel 1 μm thick GaN wires; (b) and (c) 70° and 80° tilt SEM images of 10 μm thick GaN wires; (d) and (e) cross-sectional SEM images of GaN microwires of around 10 μm thick.

GaN wire and nanodots for the incoming nutrient flux. For either 1 μm- or 10 μm-thick GaN wires, a large length-to-thickness ratio of 200 has been achieved. Given the uniform structure and electronic properties along the entire length, one single wire could be fabricated into multiple devices intrinsically connected together.[23] All the GaN wires in this work showed triangular cross sections, as illustrated in Fig. 2(c)–2(e). Most of the wires exhibited smooth and symmetrical side walls which are identified as GaN semi-polar planes, $(10\bar{1}1)$ and $(01\bar{1}1)$, according to their angles with respect to the substrate. The naturally evolved GaN $\{10\bar{1}1\}$ planes are ideal for growing semi-polar InGaN/GaN multi-quantum wells (MQWs) with reduced quantum-confined stark effect (QCSE) compared with conventional polar ones.[24,25] Fig. 2(e) shows the cross-sections of six parallel wires with thickness of $\sim$10 μm. All the GaN wires in this image showed similar geometry, indicating uniform GaN wire growth through crack-induced nucleation. Considering the nucleation of GaN wires greatly relied on the cracks in the nanoporous SiO_2 film, further thinning down the SiO_2 film thickness and intentionally inducing some thermal stress will help generate more crack-lines in the nanoporous SiO_2 film and increase GaN wire density.

In order to determine the stress status and assess the crystal quality of GaN wires grown on Si substrate, micro-Raman scattering spectra were collected from a 10 μm-thick wire from both [0001] and $[11\bar{2}0]$ directions [Fig. 3]. A 514.5 nm line of an Ar+ laser was used as the excitation source and the spot diameter of the focused laser beam on the sample was about 1.5 μm using a 100× objective. In the Raman spectrum obtained along [0001] [Fig. 3(a)], in addition to the Si substrate peak at 520 cm^{-1}, a prominent GaN E_2 (high) peak is observed at 566.5 cm^{-1}, which is very close to the same E_2 (high) emission peak position in stress-free GaN bulk material (567.5 cm^{-1}).[26] This indicates that the GaN wires are nearly or fully relaxed in spite of lattice and thermal mismatch with the Si substrate. Since GaN wires have very small footprints on the GaN/Si template underneath, the overgrown structure experiences minimal thermal stress from the substrate during temperature ramp-down. The linewidth of the wire E_2(high) peak was only 5.3 cm^{-1}, indicating a homogeneous and low defect structure in the GaN wire. When probing along $[11\bar{2}0]$, a greatly diminished or even no E_2 (H) signal was observed for crossed or parallel polarization detection, as seen in Figs. 3(c) and 3(b), respectively. These two spectra confirmed that the GaN wire c-axis is perpendicular to the (111) Si substrate according to the selection rules for wurtzite structure.

The wires nucleate on a GaN template, which is known to possess a high dislocation density. Cross-sectional TEM was utilized to evaluate crystal properties of the microstructure and to determine the extent to which these preexisting dislocations propagate into the wires. GaN wire samples were prepared using conventional mechanical thinning followed by ion beam milling. All TEM analyses were carried out on a JEOL2010F field-emission microscope operating at 200 keV. Taken near the $\langle 11\bar{2}0\rangle$ zone axis, Fig. 4(a) presents the cross section of a wire grown on the nanoporous SiO_2 template. The selective area diffraction (SAD) pattern [inset

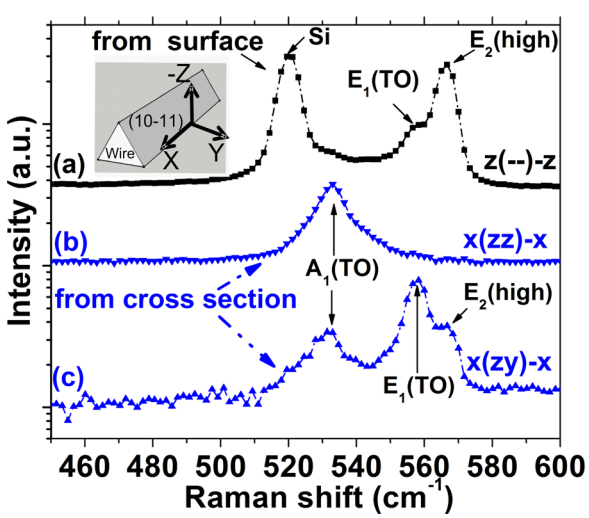

FIG. 3. Micro-Raman spectra of 10-μm-thick GaN wires observed from surface and cross section.

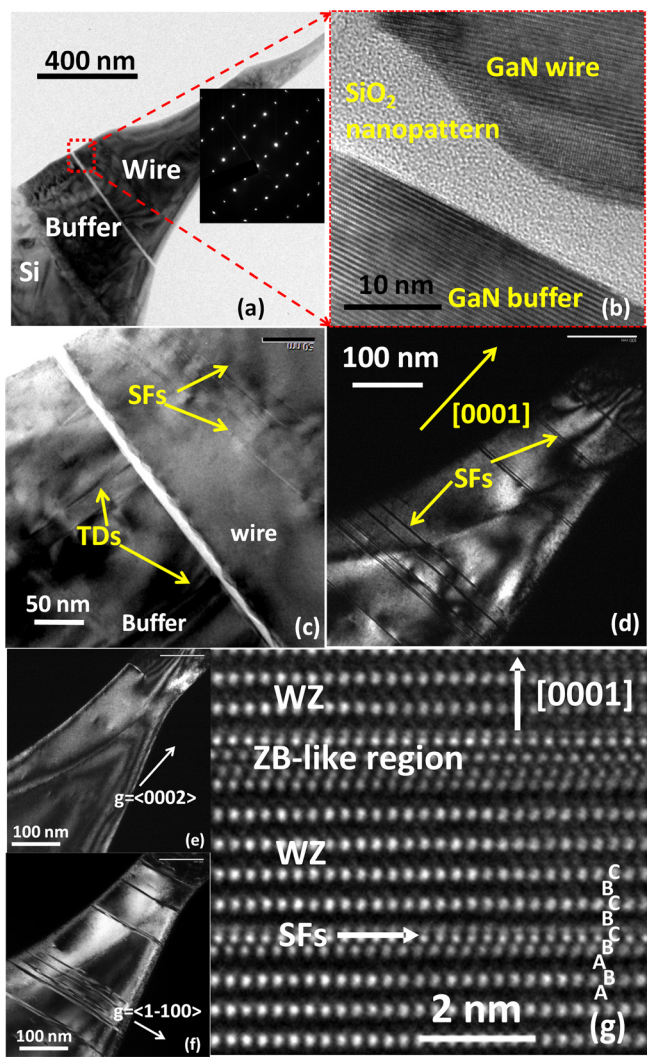

FIG. 4. (a) Low-resolution TEM image of a portion of a GaN wire (inset: SAD using $\langle 11\bar{2}0\rangle$ zone axis); (b) HRTEM image of GaN wire near the nanoporous SiO_2 film; (c) bright-field image showing defects in the GaN buffer and wire; (d) multi-beam dark-field image showing SFs in the 1 μm thick position of GaN wire; (e) and (f) two-beam dark-field images of SFs using two perpendicular **g** vectors; (g) HRTEM images displaying two kinds of stacking disorders in the GaN wires.

of Fig. 4(a)] and high-resolution (HR) image [Fig. 4(b)] reveal that the GaN microwires have a single-crystalline wurtzite structure. The GaN wire (0001) plane is parallel to the Si (111) plane, which is consistent with the observation that GaN wire c-axis is perpendicular to Si (111) plane from the polarized micro-Raman spectra. It can be found in Fig. 4(b) that lateral portion of the GaN wires which were grown over the SiO_2 mask were in a close contact with the SiO_2. The GaN wire (0001) plane tilts from rather than being strictly parallel to the GaN buffer (0001) plane. The crystallographic tilt of the GaN wire (~12.4°) could be possibly resulted from the GaN buffer crystallographic tilt in the crack area where wire regrowth started. The GaN buffer is populated with threading dislocations (TDs), however, only some striations parallel to the GaN wire c-plane appear in the GaN wire above nanoporous growth template, as shown in Fig. 4(c). The striation density decreases at regions further away from the mask layer [Fig. 4(d)]. The horizontal line features are identified as stacking faults (SFs) along c-axis of the wurtzite crystal, as seen in the HR-TEM images in Fig. 4(g). A low density of cubic GaN inclusions were observed in agreement with the streak-free diffraction spots in the SAD pattern [inset of Fig. 4(a)]. The SFs continue from one end to another in the observed area without any termination or association with partial dislocations. In two-beam dark-field analysis, the SFs vanish for $\mathbf{g} = \langle 0002 \rangle$ [Fig. 4(e)] and are clearly visible for $\mathbf{g} = \langle 1\bar{1}00 \rangle$ [Fig. 4(f)]. Since no additional SFs were observed when switching from $\mathbf{g} = \langle 1\bar{1}00 \rangle$ to $\mathbf{g} = \langle 1\bar{1}01 \rangle$, it is established that the observed SFs are intrinsic in nature.[27] Fig. 4(g) illustrated two kinds of stacking disorders inside the horizontal GaN microwires. The bottom stacking disorder revealed that the stacking order of ABAB along the c axis of wurtzite GaN was altered to ABABCBCB in the faulted area. The top stacking fault showed a local deviation from the hexagonal wurtzite (0001) stacking sequence to the cubic zinc blende (111) stacking sequence. The formation of SFs can be related to the fast GaN wire growth rate along c-axis and also the presence of certain impurities during the growth which can perturb the growth.[28,29] With improvements in the substrate preparation and optimization of the growth procedure, reductions in the SF density for wires monolithically grown on silicon should be achievable.

The electrical properties of un-doped GaN wires were measured using a standard probe-station after ultraviolet photolithography, metal deposition (Ti/Al/Ni/Au), lift-off, and annealing. The GaN wire resistivity, ρ, was derived by $\rho = RA/L$, where R is the resistance calculated by the I-V measurement, A is the cross-sectional area of GaN wire, and L is the distance between contacts. As shown in Fig. 5, the GaN wires exhibited high conductivity, and the resistivity was in the range of 20–30 mΩ cm, regardless of the GaN thickness (1 μm or 10 μm thick), which indicated that surface-related conduction played a negligible role in the resistivity measurement. Temperature-dependent resistance measurements were also performed for the 1 μm thick wire, as shown in Fig. 5. At all the measurement temperatures, ohmic current-voltage characteristics were observed. With metal pad distance of 16 μm, the measured wire resistance steadily increased from 1141 Ω at 300 K to 4973 Ω at 70 K,

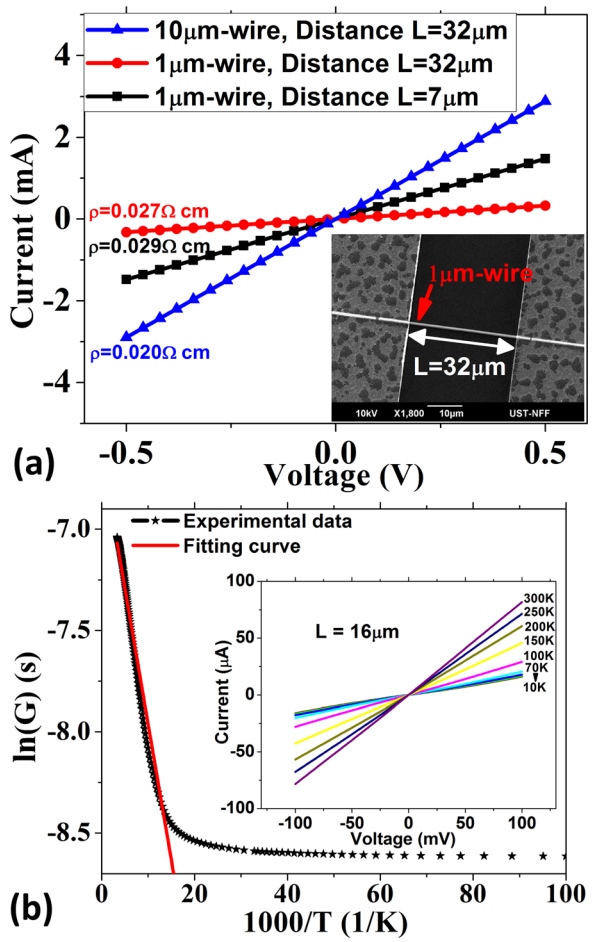

FIG. 5. (a) Ohmic I-V characteristics of GaN wires of different sizes by two-probe measurements; (b) conductance as a function of temperautre for 1 μm thick wire using four-probe configuration, inset: temperature-dependent I-V curves.

but possessed a weak dependence for temperatures from 70 K (4973 Ω) to 10 K (5513 Ω), as shown in the inset of Fig. 5(b). A fitting of the temperature-dependent conductance yields a thermal activation energy of $E_a = 12.8$ meV according to $G(T) \sim \exp(-E_a/k_BT)$, where G(T) is temperature-dependent conductance and k_B is the Boltzmann constant. The relatively small thermal activation energy and resistance flattening at very low temperature (10 K to 50 K) implied impurity band conduction.[30] Considering the measured E_a being 12.8 meV and the presence of the Si substrate, Si (activation energy between 12 meV and 17 meV in GaN[31]) was regarded to be the electron donors in the regrown wires, although the GaN wires were grown without intentional doping. According to the wire resistivity, the carrier density was estimated to $1 \times 10^{18}\,\mathrm{cm}^{-3}$ (Ref. 32 and references therein), given the micrometer scale of the measured horizontal wires.

In summary, in-plane GaN microwires were grown on nano-scale porous SiO_2 patterned GaN/Si templates by MOCVD. Well-aligned GaN microwires were grown along the three equivalent $\langle 11\bar{2}0 \rangle$ directions and were nucleated at cracks within a 20-nm thick SiO_2 template layer. All the GaN wires exhibited triangular cross-sections, which were enclosed by (0001), $(10\bar{1}1)$, and $(01\bar{1}1)$ planes. The length and thickness of the GaN microwires could be controlled by growth time while length-to-thickness ratio could be as high

as 200. Micro-Raman and cross-sectional TEM analysis confirmed that the wires were predominantly wurtzite with a low or unmeasurable dislocation density and a low density of intrinsic SFs. The regrown GaN microwires exhibited very low resistivity of 20–30 mΩ cm at room temperature, which is independent of wire thickness. Temperature-dependent measurement implied unintentional impurity was the main reason for high carrier density inside the wires with thermal activation energy of 12.8 meV. With further optimization in heterostructure design and doping profiles, the long horizontal GaN microwires would be an ideal platform for semi-polar LEDs and III-nitride based transistors directly integrated with silicon technologies.

This work was supported in part by the Research Grants Council (RGC) theme-based research scheme (TRS) of the Hong Kong Special Administrative Region Government under Grant No. T23-612/12-R. The authors gratefully acknowledge use of facilities and instrumentation supported by the University of Wisconsin Materials Research Science and Engineering Center (DMR-1121288). The authors would like to thank Professor P. Sheng and Q. H. Chen in the Physics Department of HKUST for providing temperature-dependent measurements and technical assistance. The authors would also like to thank K. W. Ng and K. H Tam for many fruitful discussions.

[1]F. Qian, S. Gradečak, Y. Li, C. Y. Wen, and C. M. Lieber, Nano Lett. **5**(11), 2287 (2005).
[2]Y. L. Chang, J. L. Wang, F. Li, and Z. Mi, Appl. Phys. Lett. **96**(1), 013106 (2010).
[3]S. Gradečak, F. Qian, Y. Li, H. G. Park, and C. M. Lieber, Appl. Phys. Lett. **87**(17), 173111 (2005).
[4]S. Vandenbrouck, K. Madjour, D. Theron, Y. Dong, Y. Li, C. M. Lieber, and C. Gaquiere, IEEE Electron Device Lett. **30**(4), 322 (2009).
[5]P.-M. Coulon, M. Hugues, B. Alloing, E. Beraudo, M. Leroux, and J. Zuniga-Perez, Opt. Express **20**(17), 18707 (2012).
[6]J. Ahn, M. A. Mastro, P. B. Klein, J. K. Hite, B. Feigelson, C. R. Eddy, and J. Kim, Opt. Express **19**(22), 21692 (2011).
[7]C. C. Chen and C. C. Yeh, Adv. Mater. **12**(10), 738 (2000).
[8]C. Chèze, L. Geelhaar, O. Brandt, W. M. Weber, H. Riechert, S. Münch, R. Rothemund, S. Reitzenstein, A. Forchel, T. Kehagias, P. Komninou, G. P. Dimitrakopulos, and T. Karakostas, Nano Res. **3**(7), 528 (2010).
[9]J. Su, G. Cui, M. Gherasimova, H. Tsukamoto, J. Han, D. Ciuparu, S. Lim, L. Pfefferle, Y. He, A. V. Nurmikko, C. Broadbridge, and A. Lehman, Appl. Phys. Lett. **86**(1), 013105 (2005).
[10]J. Zhang, X. S. Peng, X. F. Wang, Y. W. Wang, and L. D. Zhang, Chem. Phys. Lett. **345**(5–6), 372 (2001).
[11]J. E. Allen, E. R. Hemesath, D. E. Perea, J. L. Lensch-Falk, Z. Y. Li, F. Yin, M. H. Gass, P. Wang, A. L. Bleloch, R. E. Palmer, and L. J. Lauhon, Nat. Nanotechnol. **3**(3), 168 (2008).
[12]Q. Li, J. B. Wright, W. W. Chow, T. S. Luk, I. Brener, L. F. Lester, and G. T. Wang, Opt. Express **20**(16), 17873 (2012).
[13]S. A. Fortuna and X. Li, Semicond. Sci. Technol. **25**(2), 024005 (2010).
[14]D. Tsivion, M. Schvartzman, R. Popovitz-Biro, P. von Huth, and E. Joselevich, Science **333**(6045), 1003 (2011).
[15]J. W. Yu, P. C. Yeh, S. L. Wang, Y. R. Wu, M. H. Mao, H. H. Lin, and L. H. Peng, Appl. Phys. Lett. **101**(18), 183501 (2012).
[16]C.-K. Li, P.-C. Yeh, J.-W. Yu, L.-H. Peng, and Y.-R. Wu, J. Appl. Phys. **114**(16), 163706 (2013).
[17]Z. Wu, M. G. Hahm, Y. J. Jung, and L. Menon, J. Mater. Chem. **19**(4), 463 (2009).
[18]R. Dowdy, D. A. Walko, S. A. Fortuna, and Li Xiuling, IEEE Electron Device Lett. **33**(4), 522 (2012).
[19]X. Zou, K. M. Wong, W. C. Chong, J. Ma, and K. M. Lau, Phys. Status Solidi C **11**(3-4), 730 (2014).
[20]E. Han, K. O. Stuen, M. Leolukman, C.-C. Liu, P. F. Nealey, and P. Gopalan, Macromolecules **42**(13), 4896 (2009).
[21]F. K. Thomas and J. M. Luke, J. Phys. D **43**(18), 183001 (2010).
[22]G. Liu, H. Zhao, J. Zhang, J. Park, L. J. Mawst, and N. Tansu, Nanoscale Res. Lett. **6**(1), 342 (2011).
[23]W. Il Park, G. Zheng, X. Jiang, B. Tian, and C. M. Lieber, Nano Lett. **8**(9), 3004 (2008).
[24]G. You, J. Liu, Z. Jiang, L. Wang, N. A. El-Masry, A. M. Hosalli, S. M. Bedair, and J. Xu, Opt. Lett. **39**(6), 1501 (2014).
[25]H. Zhong, A. Tyagi, N. N. Fellows, F. Wu, R. B. Chung, M. Saito, K. Fujito, J. S. Speck, S. P. DenBaars, and S. Nakamura, Appl. Phys. Lett. **90**(23), 233504 (2007).
[26]C. Kisielowski, J. Krüger, S. Ruvimov, T. Suski, J. W. Ager, E. Jones, Z. Liliental-Weber, M. Rubin, E. R. Weber, M. D. Bremser, and R. F. Davis, Phys. Rev. B **54**(24), 17745 (1996).
[27]T. Y. Liu, A. Trampert, Y. J. Sun, O. Brandt, and K. H. Ploog, Philos. Mag. Lett. **84**(7), 435 (2004).
[28]S. Khromov, C. G. Hemmingsson, H. Amano, B. Monemar, L. Hultman, and G. Pozina, Phys. Rev. B **84**(7), 075324 (2011).
[29]S. Khromov, B. Monemar, V. Avrutin, H. Morkoç, L. Hultman, and G. Pozina, Appl. Phys. Lett. **103**(19), 192101 (2013).
[30]J. Moesslein, A. Lopez-Otero, A. L. Fahrenbruch, D. Kim, and R. H. Bube, J. Appl. Phys. **73**(12), 8359 (1993).
[31]W. Goütz, N. M. Johnson, C. Chen, H. Liu, C. Kuo, and W. Imler, Appl. Phys. Lett. **68**(22), 3144 (1996).
[32]P. Tchoulfian, F. Donatini, F. Levy, B. Amstatt, P. Ferret, and J. Pernot, Appl. Phys. Lett. **102**(12), 122116 (2013).